Parameters Optimization Of DC Voltage Margin Controllers Based on VSC-MTDC

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Abstract— **In this paper, a simplex algorithm to optimize the parameters of DC voltage margin controllers in a voltage source converters multi-terminal direct current (VSC-MTDC) system is proposed. The proposed approach presents a multi objective function with different time intervals using integral of time-weighted square of the error (ITSE), such that the voltage margin controllers will provide a minimum undershoot, minimum overshoot and fast settling time performance. The performance of the proposed approach is tested and examined on a three terminal VSC-MTDC system in PSCAD environment through time domain simulations.**

***Index Terms*— VSC-MTDC, DC voltage margin, simplex algorithm, optimization, ITSE.**

I. Introduction

With the increasing global demand of energy and environmental changes, more and more countries are paying attention to clean and renewable energy. However, several sites for exploitation of renewable resources are usually remotely located from demand centers. Facing this situation, the research community is putting a considerable effort and it is witnessing the development of direct current technology systems over the last recent years. Dc technology possesses many advantages related to the issue of how to efficiently transmit electrical energy over long distances [1-4]. Scholars from research institutions and power industry all over the world are holding the viewpoint that the novel MTDC technology based on voltage source converter (VSC), possesses great advantages in reliability improvement, in energy trading between regions, in maintenance and in independent control of active and reactive power [5-8]. The Nan'ao HVDC project involving China Southern Grid, which was initially a three-terminal system and commissioned in late 2013, is the first MTDC system based upon VSC technology [9].

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Inside a VSC-MTDC network, direct voltage control is certainly one of the most important tasks given to VSC-HVDC stations. A well-controlled direct voltage on a HVDC grid requires a balanced power flow between all the interconnected stations [5]. Numerous papers investigated the coordinate control method of dc voltage, however, dc voltage control based voltage margin method and voltage droop methods are the ones mostly employed in literatures[6],[10-15].

Very few papers addressed the quantitative and qualitative PI parameters optimization of dc voltage controllers. Proportional gains adjustments vary the bandwidth to meet the settling time specification, and integral time constant are normally used to reduce steady state error [16]. The most HVDC systems practices often select PI parameters based on operator's experience[13],[17]. Recently, intelligent optimization algorithm like PSO [18-20], genetic algorithm [21], simplex algorithm [22] been used to address this issue in MTDC system, but most of them focused on single converter stations optimization and used integral of time-weighted absolute value of error criterion. In [23], simplex algorithm approach has been used on a 3 terminals voltage droop controlled VSC-MTDC system using a single objective function optimization process; however some deficiencies appeared with the optimization of only one station converters. In [24], ISE (Integral square error) index has been suggested, but not implemented to mitigate dc voltage fluctuation and long active power time response issues.

In spite of good results of such papers, there are still some shortcomings in simultaneously addressing the issue of fast dc voltage control at VSC level and the issue of fast-coordinated dc voltage control at VSC-MTDC level. In this paper a simplex algorithm is adopted to optimize the PI parameters of voltage margin controllers in a VSC-MTDC system. Also a multi

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-objective function with different time intervals using ITSE is defined such that the voltage margin controllers will provide a minimum undershoot, minimum overshoot and fast settling time performance. The performance of the proposed approach is tested and examined on a three terminal VSC-MTDC system in PSCAD environment through time domain simulations under transient and steady state.

II. Modeling and Control of VSC-MTDC Grids

VSC-MTDC grids are characterized by the interconnection of more than 2 VSC systems. The control of MTDC grids includes DC voltage regulation at DC terminals, control of active and reactive power at the point of common coupling, and maintaining the PCC's AC voltage.

The most commonly used control strategy for the VSC stations is based on the vector control [5],[12],[25]. So by employing full controlled electronic IGBT, modulation technique and vector control, the VSC station can carry out a decoupled control of the active and reactive power as well as the DC and AC voltage flexibly. In vector control, the AC currents and voltages of the converter station (at the PCC) are transformed into the rotating direct-quadrature (d-q) reference frame, synchronized with the AC grid voltage by means of a phase-locked loop (PLL). Fig. 1 illustrates the general architecture of the vector control at a VSC-HVDC station.

A. Inner Current Controller

The inner current controller, includes fast proportional–integral (PI) controllers, which track the reference currents, set by the outer controllers, and produces the voltage reference for the converter (U_{dref}, and U_{qref}). To derive the structure of the ICC, the voltage at PCC (e_s) and converter-side voltage (u_c) are related by,

$$e_s - u_c = R_T i_c + L_T \frac{di_c}{dt} \tag{1}$$

where, i_c is the current flowing from the AC grid to the converter, and R_T and L_T represent the total resistance and inductance between the PCC and converter. Then by applying the Park transformation, (1) can be expressed in d-q reference frame by,

$$e_d - u_d = R_T i_d + L_T \frac{di_d}{dt} - \omega L_T i_q \tag{2}$$

$$e_q - u_q = R_T i_q + L_T \frac{di_q}{dt} - \omega L_T i_d \tag{3}$$

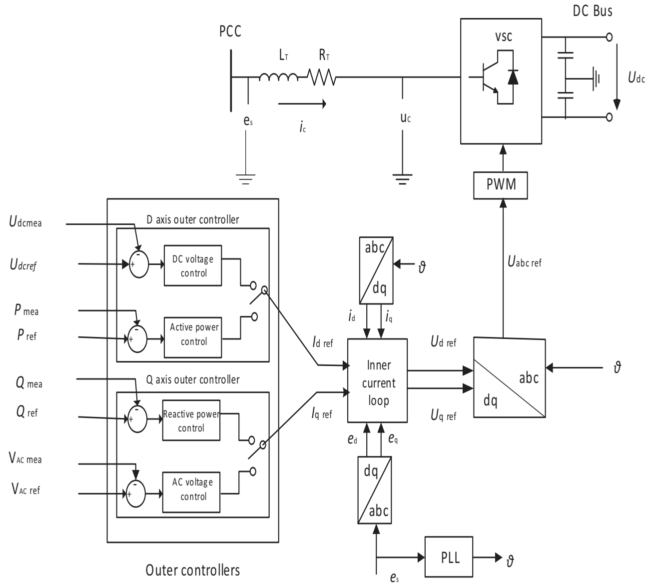

Fig.1. Architecture of vector control at a VSC station

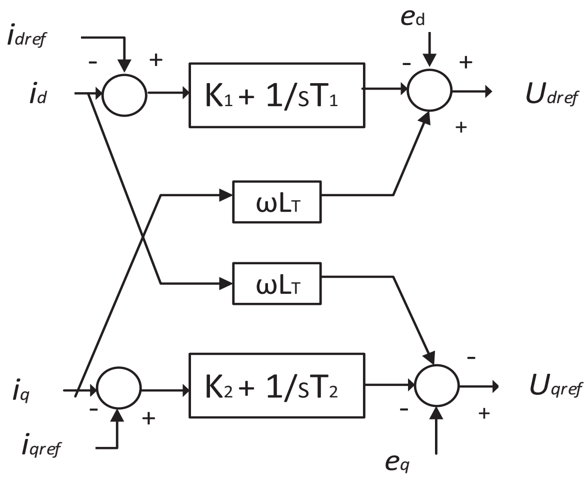

Fig.2. Structure of the Inner Current Controller

Where ω is the angular frequency of the AC voltage at the PCC. The structure of the ICC is obtained using (2)-(3) and is shown in Fig. 2. The reference voltages ($\mathrm{U_{dref}}$) and $\mathrm{U_{qref}}$) are then transformed back into the *abc* reference frame and used to generate the switching signals for the converter.

B. Outer controller

The outer controllers are responsible for generating the reference currents for the inner current controller (I_{dref} and I_{qref}) and they include the active and reactive channels, as shown in Fig. 1. The active channels are responsible for regulation of the active power or DC voltage while the reactive channels control the reactive power or amplitude of AC voltage at the PCC. For active power control, the power equations in d-q reference frame can be used,

$$P = u_d i_d \tag{4}$$

$$Q = -u_d i_q \tag{5}$$

To maintain the DC voltage at its reference value, the active power exchanged with the AC grid must be properly regulated. Hence, modification of the d-axis current (i_d) allows controlling the DC voltage within the permissible limits.

III. Simplex Algorithm and Objective Function

A. The ITSE Index

There are many minimum error indexes being used to measure the performance of control systems. ITSE (Integral of Time-weighted Square of the Error) is one of these indexes. It can be expressed as (6)

$$J_{ITSE} = \int_0^T t.e^2(t).dt \tag{6}$$

Where $e^2(t)$is the function of the error of control variables (e.g. DC voltage, active power, reactive power) compared with the references and the upper limit T is a finite time chosen so that the integral approaches a steady-state value. Voltage margin block diagram is shown in Fig.3.

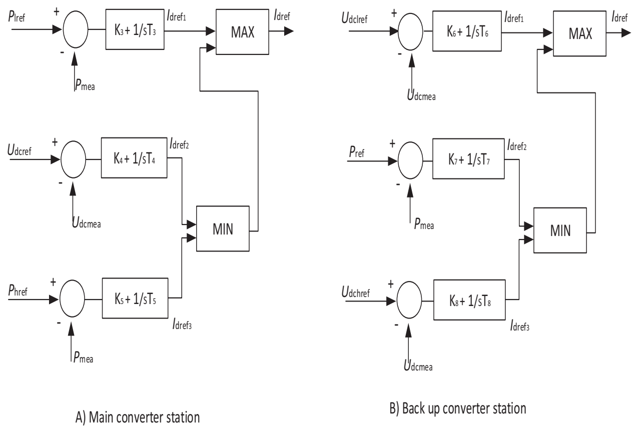

Fig.3. Voltage Margin Method control block diagram

B. Simplex Algorithm

The nonlinear-Simplex method of Nelder and Mead is a heuristic optimization method based on geometric considerations. The geometric figure whose vertices are defined by a set of *n+1* in a n-dimensional space is called a simplex. The basic idea in the simplex method is to compare the value of the objective function at the n+1 vertices of a simplex, not seek the optimum point in a direction. The method discards the worst vertex, i.e. highest value for a minimization problem, a new vertex is chosen and gradually toward the optimum point during the iterative process [22-23].

C. Objective Function

Compared to most of the papers that uses single objective function, this paper uses a multi-objective function divided into several time intervals where there is an active power step change for each time interval. Through this method, the system will be subjected to different operating conditions during the optimization process in order to find the optimal PI controller's parameters that will minimize the DC voltage, active and reactive powers errors. But because our VS-MTDC possesses several control loops the objective function will be to minimize the weighted sum of ITSE. The corresponding objective function can be expressed in (7) and (8),

$$O_f(X) = \sum_{i=1}^{n} m_i f_i(X) \tag{7}$$

$$f_i(X) = \sum_{j=1}^{m} \omega_j ITSE_j = \sum_{j=1}^{m} \omega_j \int_0^T t.e^2(t).dt \tag{8}$$

Where f_i is the performance index for the i^{th} sub-objective, m_i is the weighting factor applied to the i^{th} sub-objective. ω_j is the weighting factor corresponding to the j^{th} controlled variables. m is the number controlled variables. n is the number of time intervals. Vector X=(X_1 X_2 … X_n) is the control system parameters, i.e. PI parameters.

D. Simplex algorithm for optimization of DC Voltage Margin Controllers

Several methods like trial and error [23] method or classical frequency response method [26] been used to determine the initial PI parameters values of a VSC. So in this paper the initial value are known [27]. The multi-objective function used in this paper focuses on minimizing the ITSE index related to dc voltage, active power and reactive power. Based on the overall control strategy as seen in Fig.3 and Fig.5, there are 10 PI controllers in the three terminal, but because the structure of the reactive power controller (Q_{ref}) of each converter station is the same, in order to simplify the calculation, the number of PI controllers that will be optimized been reduced to 8. Knowing that each PI controllers holds 2 parameters (K_j and T_j), the simplex algorithm will moves the initial PI parameters values toward the optimum one's , which will makes a minimum objective function value through iterative process, known as reflection, contraction, and expansion [22]. Thus the (X) in (7) and (8) will be a set of parameters of outer loops control of $\mathrm{VSC_1}$, $\mathrm{VSC_2}$, and $\mathrm{VSC_3}$. Then, based on (7), (8), the active power steps changes and the fact that $m_i = 8$ during the optimization process, the objective function for the MTDC system is given by:

$$\begin{aligned} O_f(X) &= \sum_{j=1}^{5} 8.f_i(X) \\ &= \sum_{j=1}^{8}\omega_j\int_0^{t_1} t.e^2(t).dt + \sum_{j=1}^{8}\omega_j\int_{t_1}^{t_2} t.e^2(t).dt + \ldots + \sum_{j=1}^{8}\omega_j\int_{t_4}^{t_5} t.e^2(t).dt \end{aligned} \tag{9}$$

In this paper, all the weighting factors corresponding to the controlled variables (ω_j) are equal to one, except the one's corresponding to the DC voltage variable which is equal to two. The flow chart of the process for parameters optimization is shown in Fig.4.

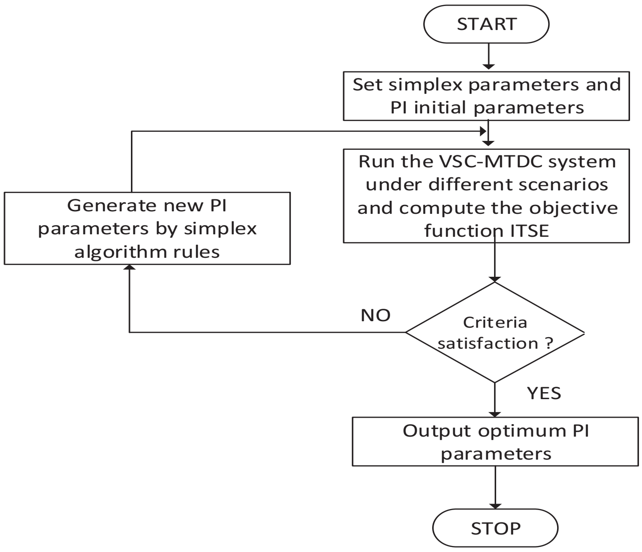

Fig.4. Flow chart of optimization process

IV. Simulation Studies

A. Three-terminal VSC-MTDC

In order to verify the effectiveness of our optimal coordinated approach, a three–terminal VSC-MTDC system is built in PSCAD simulation software. And the structure of the system is shown in Fig.5. The test system is composed of three AC grids with terminal voltage of 10kV, the frequency is 50Hz, the transformers connection are 10kV/5kV, the rated voltage of the MTDC grid is 10kV, and the DC line resistance been neglected.

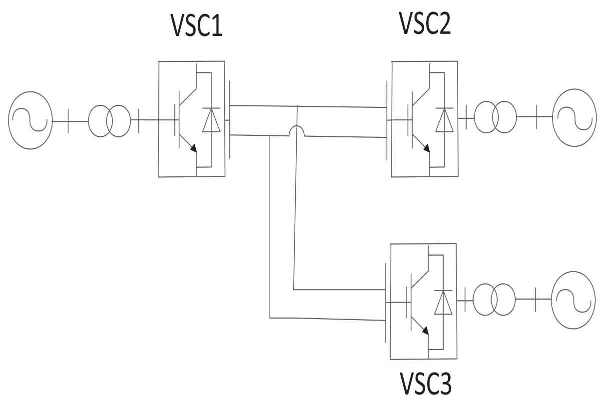

Fig.5. Structure of three-terminal VSC-MTDC

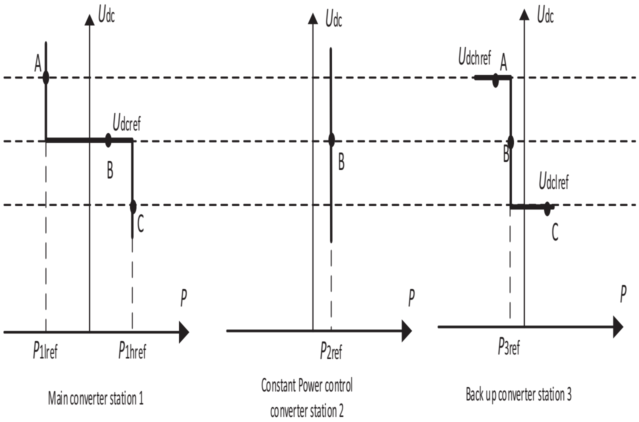

Fig.6. Three-terminal VSC-MTDC Voltage Margin Method P-U_{dc} characteristics curves

In Fig.6, VSC_1 and VSC_3 take DC voltage margin control as the outer loop control. VSC_2 take constant active power control as the outer loop control. The control characteristics of the three converters stations are shown in Fig.6, of which, U_{dcref} = 10kV, P_{1lref} = -4MW, P_{1href} = 4MW, P_{3ref} = -2MW, U_{dclref} = 9.5kV, U_{dchref} = 10.5kV.

B. The Results of Simulation

During the optimization process the system is subjected to 4 steps change of active power in order to experience overvoltage and under voltage operating conditions: at t =1s , the P_{2ref} changed from 7MW to 2MW, at t=2s, it changed from 2MW to -6MW, at t=3s it changed rom -6MM to 2MW and at t=4s, it changed from 2MW to 7MW. The table I show a comparison between initial and optimal parameters, plus their related objective function values.

Table I. Comparison between initial and optimized parameters and objective function value

VSC stations	Controllers loop	Initial K_j	Initial T_j	Optimal K_j	Optimal T_j
	U_{dcref}	10	0.0025	10	0.0047
VSC_1	P_{1lref}	0.001	0.005	0.0010	0.0051
	P_{1href}	0.001	0.005	0.0010	0.0051
VSC_2	P_{2ref}	0.001	0.01	0.002	0.00042
	P_{3ref}	0.01	0.01	0.097	0.00094
VSC_3	U_{dclref}	5	0.0025	5	0.00022
	U_{dchref}	5	0.0025	5	0.000049
$VSC_{1,2,3}$	Q_{ref}	0.01	0.01	0.01	0.082
Objective Function Value		0.49		0.15	

From Table I, it can be seen that the value of ITSE value is about 70% much smaller after optimization process, which rudely shows the effectiveness of our optimization algorithm.

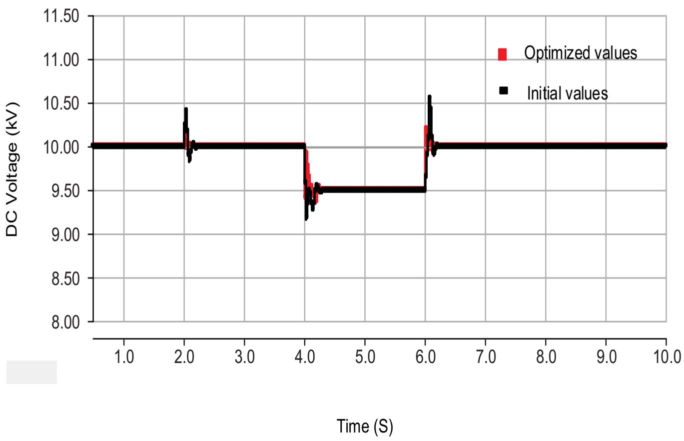

Fig.7. DC voltage response during active power step changes

Fig.7 illustrates the system dynamic DC voltage response subjected to VSC_2 active power step changes (Fig.8). At t =2s the P_{2ref} changed from 1MW to 5MW, at t =4s it changed from 5MW to -2MW, at t =6s it changed from -6MW to 1MW. As revealed in Figure 8, the optimal coordinated control parameters obtained by the proposed method can control the system more accurately, and can complete the smooth switching of the system when the power changes. The system DC voltage is stable and accurate in steady state, and the control effect is good.

In order to verify the robustness of our approach, the system dynamic response while the main converter station is remove from service at t =1s been analyzed and compared. The DC voltage and active powers are shown in Fig.9-11.

When t =1s, VSC_1 is out of service, the DC system is lacking active power and the DC system voltage drops.

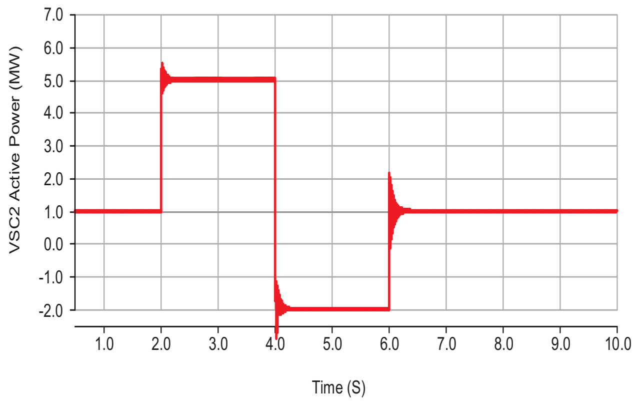

Fig.8. VSC_2 Active power step changes

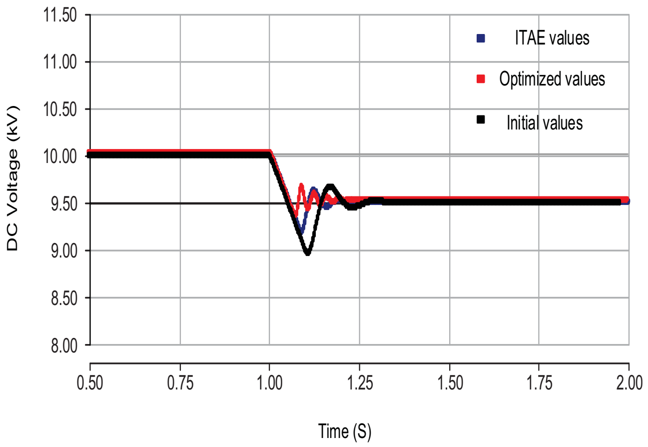

Fig.9. DC voltage response after VSC_1 is out of service

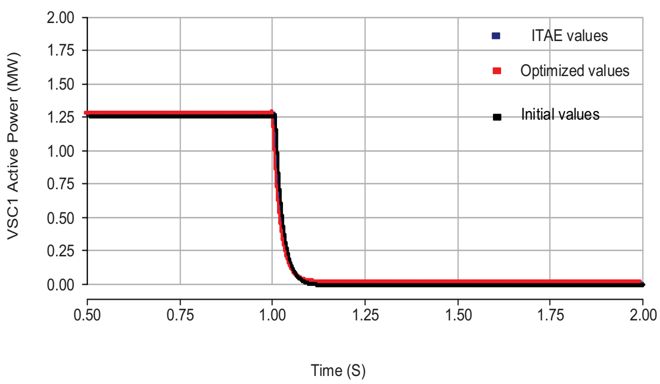

Fig.10. VSC_1 Active power

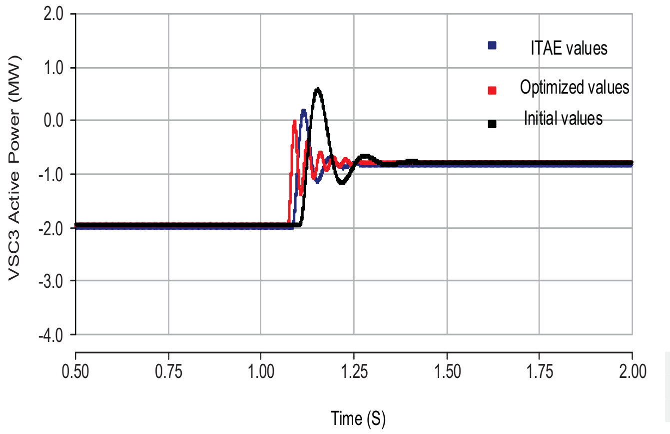

Fig.11. VSC_3 Active power after VSC_1 is out of service

When the voltage drops to the lower limit U_{dclref} = 9.5kV, VSC_3 is switched from the original active power control to the constant voltage control, the DC voltage is quickly stabilized at 9.5kV, quicker than using initial parameters values and also using ITAE [27]. VSC_3 Active power is also quickly adjusted to balance the system power shortage. The transition process to a new stable state is fast and the robustness of our approach is verified. The table II shows the different control strategies performance comparison when VSC_1 is out of service.

TABLE II. Performance Comparison

	DC voltage undershoot	**VSC_3** Active power overshoot	Dc voltage settling time
Initial values	0.049	1.3	1.27
Optimal values with ITAE	0.031	0.95	1.18
Optimal values	0.015	0.93	1.18

V. Conclusion

In this paper, the simultaneously issues of fast dc voltage control at VSC level and fast-coordinated dc voltage control at VSC-MTDC level been addressed using a multi objective function with different time intervals based on ITSE (integral of time-weighted square of the error) been proposed such that the optimal PI parameters of voltage margin controllers provided a minimum DC voltage deviation and better settling time performance. According to the results of simulation, the robustness of this methodology has been tested.

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