Optimal Design and Experimental Verification of FPGA-based MMC-HVDC Controller

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***Abstract*—The control system structure of modular multilevel converter based high voltage direct current (MMC-HVDC) is complicated. Data acquisition, control computation, and communication among distributed controllers lead to long link delay. The delay will further cause deterioration of the system's dynamic characteristics and even instability. This paper presents an integrated controller design based on field programmable gate array (FPGA). The parallel features of FPGA are fully utilized to complete the control calculation task and shorten the link delay as much as possible. Based on the real-time digital simulator (RTDS) platform, hardware-in-the-loop experiments are carried out to verify the function of the designed controller. The results show that the designed controller has short link delay and fast response speed, and can be used in the testing of control strategy, control parameters optimization, and so on.**

***Index Terms*—Digital control, field programmable gate arrays, hardware-in-the-loop, modular multilevel converters**

I. Introduction

Featuring high modularity, strong scalability, and low harmonic injection characteristics, modular multilevel converter (MMC) has become a preferred topology in high voltage dc (HVDC) system compared to previous two- or three-level converter [1]-[3].

The advantage of MMC comes from its unique topology of sub-module (SM) cascading, which realizes the energy transfer between AC and DC side through charge and discharge of the capacitance dispersed in each SM. With the development of MMC-HVDC system towards higher voltage and larger capacity, the number of SMs in an MMC arm can reach hundreds, and each SM should be controlled independently, which brings too much burden to the design and implementation of MMC control system.

The excellent function of the controller is an essential guarantee for the safe and stable operation of the real project. Due to the heavy computation burden of the MMC control system, it is challenging to complete all the control functions in a single controller. Therefore, the sampling, upper-level control, and lower-level control should be grouped individually. On the one hand, such a processing method will lead to the high cost of the controller, inconvenient transportation, and harsh test environment. There are many control and protection devices and massive data communicated between different control and protection devices, which makes it challenging to reduce the control link delay [4]. The measured delay of the project can be up to 600 μs [5]. The long control link delay will not only worsen the dynamic characteristics of the MMC system but also lead to the risk of oscillation and instability.

Field programmable gate array (FPGA) is a kind of parallel chip with distributed memory, pipeline architecture, and expandable high-speed IO port. It can realize fast large-scale data communication. The real-time simulation of MMC using FPGA has developed rapidly in recent years [6], [7]. Moreover, FPGA is also used in the industrial MMC controller to drive AD sampling and transfer the measured data to the upper digital signal processor (DSP). The DSP completes the following control computation task [8]. Data communication time between FPGA and DSP is a central part of the whole link delay. With the improvement of FPGA, the integrated on-chip signal processors are increasing. So FPGA can handle some complex digital signal processing [9]. However, most of the industrial controller configuration does not make full use of this feature.

This paper designs an integrated MMC controller based on FPGA. Using a single FPGA board can implement various control strategies for a one-terminal MMC system. Parallelizing the control calculation reduces the link delay of the whole system significantly. A 201-level single terminal test system is built based on the real-time digital simulator (RTDS) platform. Power flow reversal, switching frequency optimization, and circulating current suppression on/off experiments are carried out to verify the feasibility of the controller.

The rest of this paper is organized as follows. Section II reviews the general control system structure of MMC. Section III presents the parallel design and FPGA implementation of the controller. Hardware-in-the-loop experiments are carried out to verify the function of the developed controller based on the 201-level MMC system in Section IV. Conclusions are given in Section V.

II. Control Structure of MMC-HVDC System

Fig. 1 shows the general control system structure of MMC. The system is divided into the upper-level control and lower-level control. The upper-level is composed of the power calculation, the outer loop control, and the inner loop control. The outer loop control generates the current reference, and the inner loop control drives the output current tracking the

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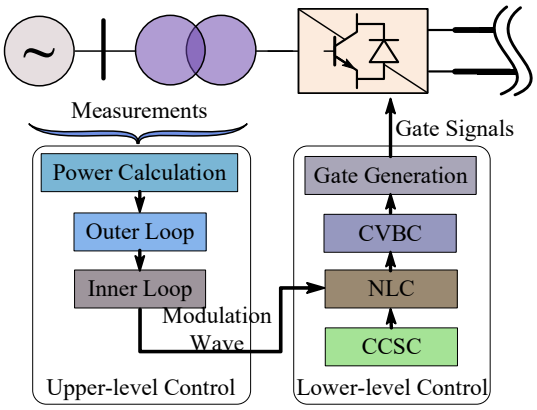

Fig. 1. General structure of MMC controller.

reference and gets the modulation wave used in the lower-level control. The lower-level includes the circulating current suppression control (CCSC), nearest level control (NLC), capacitor voltage balancing control (CVBC), and gate signal generation. The CCSC is used to eliminate the second harmonic component in the arm current to set the distribution of the internal converter energy. The NLC determines the number of SMs in each arm that need to be inserted according to the modulation wave and the CCSC output. The CVBC is used to balance the SM capacitor, making it evenly distributed. Finally, the gate signal generation link generates the gate signals for each SM and drives the SM to take corresponding actions.

III. Controller Parallel Design and FPGA Implementation

In this paper, the main idea of designing the controller is parallelization and making similar and independent control blocks work simultaneously, to reduce the control calculation time to the greatest extent. The data in this chapter are IEEE-754 standard single-precision floating-point numbers.

A. Clark Transformation

Equation (1) shows the Clark transformation taking the three-phase voltages as an example. The Clark transformation is composed of multiplication, addition, and subtraction operations realized with corresponding intellectual property (IP) cores. And the calculation diagram of Clark transformation shown in Fig. 2 is obtained. The output signal of the previous level operation is used as the input signal of the next level operation.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1}$$

B. Park Transformation

The relationship between Clark transformation and Park transformation is:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix}\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{2}$$

Thus, the Park transformation calculation diagram shown in Fig. 3 can be obtained.

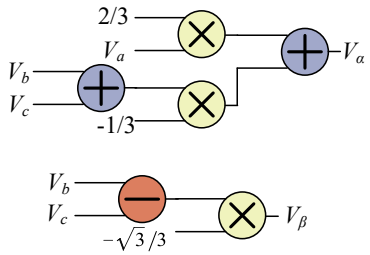

Fig. 2. Calculation diagram of Clark transformation.

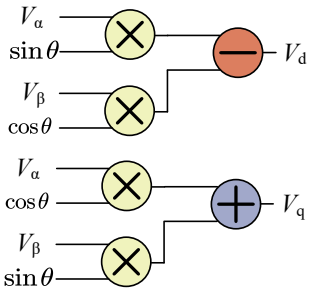

Fig. 3. Calculation diagram of Park transformation.

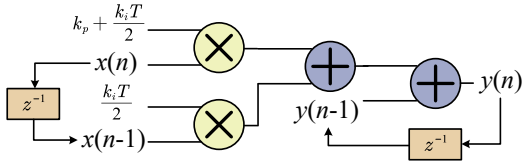

Fig. 4. Calculation diagram of PI controller.

C. PI Controller

Proportional-integral (PI) controller is a commonly used linear controller. According to the given value and the output value, the control deviation is formed. The proportion and integral of the deviation are combined to form the control quantity through linear combination. The PI controller is used in many links in the MMC control system, such as the outer loop, the inner loop, and the CCSC. The transfer function of the PI controller is

$$G_{\mathrm{PI}}(s) = k_p + k_i/s \tag{3}$$

where k_p is the proportional coefficient and k_i is the integral coefficient, respectively.

Using Tustin transformation to transform (3) form s-domain to z-domain, we can get [10]:

$$y(n) = \left(k_p + \frac{k_i T}{2}\right)x(n) + \frac{k_i T}{2}x(n-1) + y(n-1) \tag{4}$$

where T is the control period, $x(n)$ and $x(n\text{-}1)$ denote the input array, and $y(n)$, $y(n\text{-}1)$ denote the output array.

Thus, the calculation diagram of PI controller can be obtained, as shown in Fig. 4.

D. PLL

The PLL provides the grid phase reference. Fig. 5 shows its calculation diagram. The angle triangle function values are

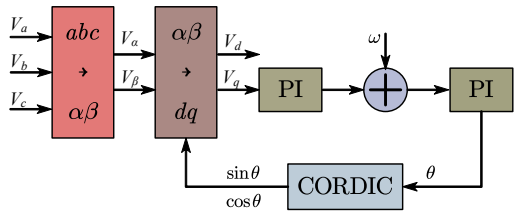

Fig. 5. Calculation diagram of PLL.

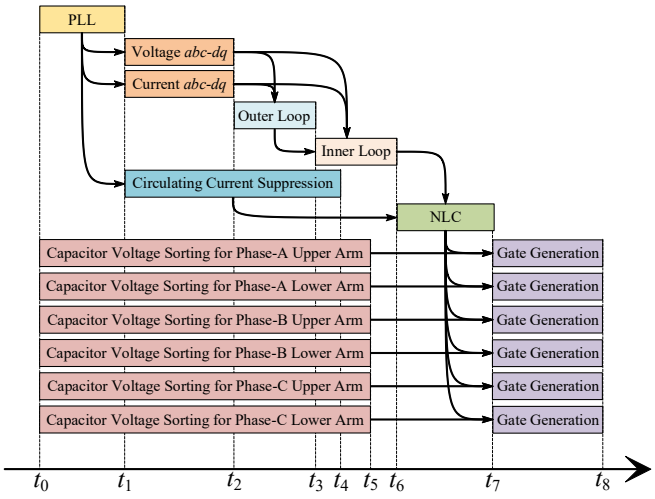

Fig. 6. Timing sequence of the controller computation.

given by the coordinate rotation digital computer (CORDIC) core available on FPGA.

E. Outer Loop, Inner Loop and CCSC

The inner and outer loops are also called vector control. In steady state, we have:

$$\begin{cases} L_s \dfrac{dI_d}{dt} = V_{sd} - V_{cd} - \omega L_s I_q \\ L_s \dfrac{dI_q}{dt} = V_{sq} - V_{cq} - \omega L_s I_d \end{cases} \tag{5}$$

The inner loop, outer loop, and CCSC depend on the previous input, so they can only be carried out in serial mode, while the calculation of the d-axis and q-axis can be carried out in parallel. Since these loops are commonly used, the control structures are not described here.

F. CVBC and Gate Generation

The DC-side terminal voltage is supported by the capacitance dispersed in each SM. And the balance of capacitor voltage is an essential premise for the stable operation of MMC [9], [11]. In this paper, we choose the bitonic sorting network to sort the capacitor voltages. The bitonic sorting network is a parallel algorithm that is easy to be implemented in FPGA [12]. The gate signals are determined according to the sorting results, the arm current direction, and the number of SMs to be inserted.

Maintaining factors are used to keep the device original state unchanged to optimize the switching frequency [13]: when the arm current is the charging direction, multiply the SM capacitor voltage that is on at the previous step by MF_1 ($MF_1 \leq 1$), and the SM capacitor voltage that is off at the previous step by MF_2 ($MF_2 \geq 1$); when the arm current is the discharging direction, multiply the SM capacitor voltage that is on at the previous step by MF_2, and the SM capacitor voltage that is off at the previous step by MF_1. After this process, the capacitor voltages are sent to the sorting network.

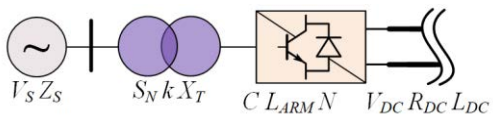

Fig. 7. Test system.

TABLE I
STUDY SYSTEM PARAMETERS

Symbol	QUANTITY	Value
S_N	transformer rated capacity (MVA)	500
k	transformer ratio (kV/kV)	230/225
X_T	transformer leakage reactance (p.u.)	0.10
V_S	rated AC-terminal voltage (kV)	230
Z_S	equivalent AC-terminal impedance (Ω)	0.1+j0.314
C	sub-module capacitance (mF)	6.6
L_{ARM}	arm inductance (mH)	50
N	number of sub-modules per arm	200
V_{DC}	rated DC-terminal voltage (kV)	±200
R_{DC}	DC transmission line resistance (Ω)	1.0
L_{DC}	DC transmission line inductance (H)	0.1

G. Timing Sequence

Fig. 6 shows the overall timing sequence of the controller. When the data acquisition is completed, the PLL and capacitor voltage sorting start. When the output of the PLL is ready, the Park transformations of voltage and current are executed in parallel. Then the outer loop control, inner loop control, and NLC are executed in sequence. The output angle of PLL can also be used for the second harmonic CCSC, so the CCSC and the Park transformation are performed synchronously. Finally, the gate signals are generated according to the NLC result and the sorting result.

The time of PLL is t_1=222 T_{clk}, the time of Park transformation is t_2-t_1=222 T_{clk}, the time of outer loop control is t_3-t_2=69 T_{clk}, the time of inner loop control is t_6-t_3=130 T_{clk}, the time of CCSC is t_4-t_1=159 T_{clk}, and the time of NLC is t_7-t_6=16 T_{clk}. Taking the MMC system with 200 SMs per arm as an example, when the parallel path number of the sorting network is 4, the time of capacitor voltage sorting is t_5=455 T_{clk}. The time of gate signal generation is t_8-t_7=100 T_{clk}. The overall calculation time is t_8=589 T_{clk}. In this paper, a 200 MHz FPGA clock is used, i.e., T_{clk}=5 ns, so the whole control calculation time is 2.945 μs.

According to the analysis above, the capacitor voltage sorting process is very time-consuming. Therefore, implementing the independent and similar control functions (such as the capacitor voltage sorting for six arms) in parallel, the control calculation time can be significantly reduced. Besides, because of the high integration of the controller designed, the data transmission is carried out in the same chip. Thus the data communication between controllers are not involved, and the link delay can be further reduced.

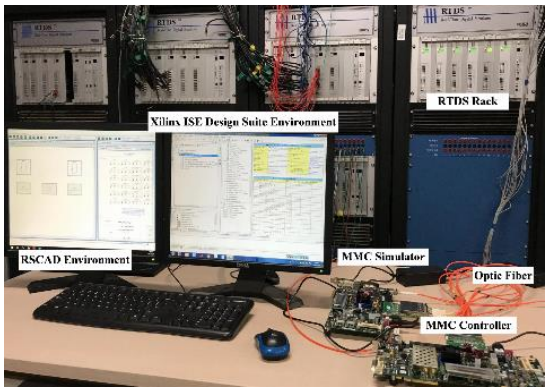

Fig. 8. Configuration of the hardware-in-the-loop experimental platform.

IV. Experimental Verification

A. Study System

A single-terminal 201-level MMC system is established in RTDS to verify the performance of the controller, as shown in Fig. 7. The system parameters are listed in Table I.

The MMC system is set to control the active and reactive power, and the reference values are 200 MW and 0 MVar, respectively. The control period is 10 μs.

B. Platform Configuration

Fig. 8 shows the hardware configuration of the experimental platform. In this paper, the Xilinx ML605 board is selected, which integrates the Virtex-6 series XC6VLX240T-1FFG1156 FPGA chip. The controller is developed in Xilinx ISE 14.7 environment using Verilog HDL. The controller design consumes 43 % register resources, 56 % LUT resources, 5 % BRAM resources, and 42 % DSP48E1 resources, respectively. The primary system runs in RTDS and FPGA-based MMC simulator [6]. The controller is connected to RTDS through optic fiber and receives the MMC operation status. The communication between the FPGA simulator and controller is also carried out through optic fiber with capacitor voltages and gate signals in a manner of bidirectional transmission.

C. Experimnetal Results

1) Power Flow Reversal: In the initial state, the active power reference value is P_{ref} = 200 MW, and the reactive power reference value is Q_{ref} = 0 MVar. When t = 0.4 s, P_{ref} is adjusted to -200 MW to realize the power flow reversal, and the changing rate is limited to 2000 MW/s. Fig. 9 shows the experimental results of the power flow reversal.

In Fig. 9, after the change of the active power reference value, the active power accurately tracks the reference under the function of the controller, while the reactive power is not significantly disturbed. The polarity of the DC component in the arm current reverses. The AC components in AC-side terminal currents and arm currents have experienced the process of changing from large to small and then to large. The system transits to a new operating point smoothly.

2) Switching Frequency Optimization: To further verify the lower-level control function of the controller, four cases are set

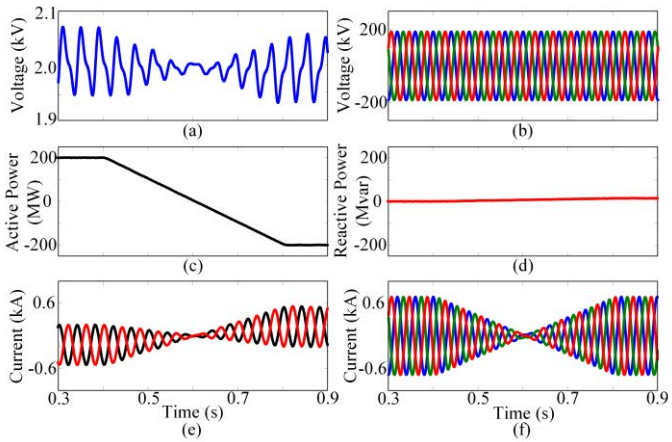

Fig. 9. Experimental results of power flow reversal. (a) Phase-A upper arm SM_1-SM_{10} capacitor voltages. (b) AC-side terminal voltages. (c) Active power. (d) Reactive power. (e) Phase-A arm currents. (f) AC-side terminal currents.

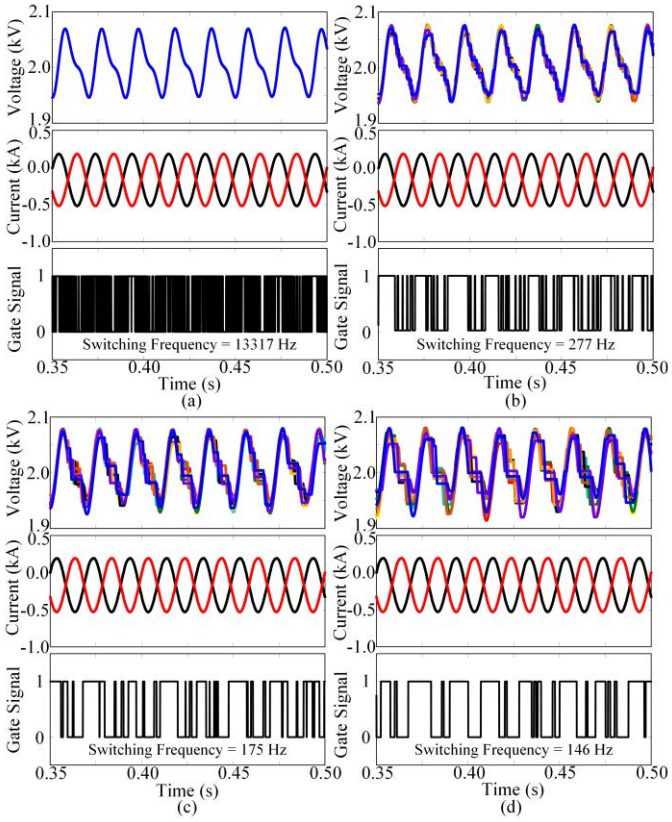

Fig. 10. Experimental results of switching frequency optimization. (a) Case I. (b) Case II. (c) Case III. (d) Case IV.

for the switching frequency optimization experiments. The maintaining factors are adjusted in each case.

- Case I: MF_1 = 1.000, MF_2 = 1.000
- Case II: MF_1 = 0.995, MF_2 = 1.005
- Case III: MF_1 = 0.990, MF_2 = 1.010

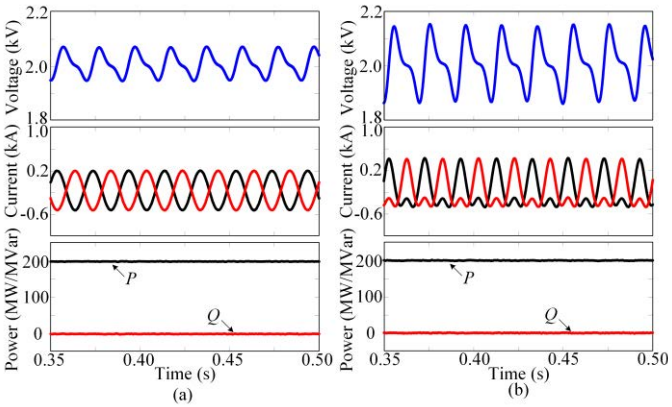

Fig. 11. Experimental results of switching frequency optimization. (a) CCSC enabled. (b) CCSC disabled.

- Case IV: $MF_1 = 0.985$, $MF_2 = 1.015$

The average switching frequency and the capacitor voltage fluctuation rate are selected to evaluate the optimization effect. The average switching frequency is defined as the sum of switching times of all SMs in a unit time divided by two times of the SM number in a single arm. The capacitor voltage fluctuation rate is the ratio of the amplitude of the fluctuation component of the capacitor voltage deviation from the rated value to the rated value.

Fig. 10 shows the corresponding experimental results under the four cases. In each case, the phase-A upper arm SM_1-SM_{10} capacitor voltages, phase-A arm currents, and phase-A upper arm SM_1 gate signal are plotted from top to bottom.

In case I, since the sorting process is carried out in every cycle, the tiny change of capacitor voltage will change the position of the SM in the sorting list. This new sorting list will result in repeated switching of the SM. The switching frequency in case I is as high as 13177 Hz. Accordingly, the capacitor voltage fluctuation in case I is the smallest, only 3.6%. In case II-IV, with the deepened optimization, the switching frequency is decreased from 227 Hz in case II to 146 Hz in case IV, and the fluctuation rate of capacitor voltage increased from 3.9% to 4.05%. It can be seen that the switching frequency can be reduced significantly without sacrificing the voltage balance by selecting the appropriate maintaining factors.

3) CCSC In and Out of Service: Fig. 11(a) and Fig. 11(b) show the experimental results when CCSC is in and out of service. From top to bottom in each figure are the phase-A upper arm SM_1-SM_{10} capacitor voltages, phase-A arm currents, and active/reactive power, respectively.

In Fig. 11(a), when the circulating current suppression controller is put into operation, the second-order harmonic in the arm currents is effectively suppressed, thus reducing the fluctuation amplitude of the capacitor voltages. Besides, the CCSC has little effect on the upper-level control, and the active power and reactive power are both accurately tracked in the two cases.

V. Conclusion

This paper presents an MMC controller designed in parallel and implemented using FPGA, and hardware-in-the-loop experiments are carried out to verify the controller functions. Several conclusions can be drawn as,

1) The designed controller is highly integrated and can flexibly realizes different modulation and control strategies. A single FPGA board can implement all control functions.

2) By parallel and integrated design of the controller, the delay caused by control calculation and data communication can be greatly reduced. The control calculation time for the 201-level MMC system in this paper is only 2.945 μs.

3) The function of the controller designed is verified by the experiments of power flow reversal, switching frequency optimization, and circulating current suppression. The controller can be used in the fields of primary parameter design demonstration, control parameter optimization, and testing of control strategies.

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