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ORIGINAL RESEARCH

# Parallel multi-rate simulation scheme for modular multilevel converter-based high-voltage direct current with accurate simulation of high-frequency characteristics and field programmable gate array-based implementation

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## Abstract

The real-time simulation of the modular multilevel converter-based high-voltage direct current (MMC-HVDC) transmission system has become a popular research topic. However, in order to meet the real-time performance, the real-time simulation technology will cause additional simulation errors for MMC-HVDC, especially on its frequency characteristics. Therefore, a parallel multi-rate simulation scheme for MMC-HVDC is developed in this work to ensure accurate simulation of high-frequency characteristics. Firstly, a non-error method based on converter transformer decoupling is proposed to decouple the converter and alternating current system; direct current transmission line decoupling and arm decoupling methods are used to achieve decoupling among and within converters. A multi-rate data synchronous mechanism is established by considering the differences among high-frequency characteristics caused by delayed data interaction. Secondly, the computing architectures of the primary system solver and modular multilevel converter controller are designed based on a field programmable gate array (FPGA). The real-time simulation platform for a four-terminal true bipolar MMC-HVDC is constructed based on the FPGA array. Thirdly, the factors in multi-rate simulation affecting the simulation accuracy of high-frequency characteristics are analysed. The simulator is shown to be accurate in steady and dynamic states. The authors also verify its applicability for further research on high-frequency resonance based on control experiments.

## 1 | INTRODUCTION

With the rapid development of power system technologies, many pieces of power electronic equipment have been put into operation and have continually increased the complexity of the systems' dynamic characteristics. Electromagnetic transient simulation has become a primary means of studying the dynamic characteristics of power electronic systems [1–3].

The modular multilevel converter (MMC) represents typical power electronic equipment used in high-voltage transmission [4–6]. For practical large-capacity MMC-based high-voltage direct current (MMC-HVDC) projects, small-step electromagnetic transient simulation has become necessary [7, 8]. However, available techniques for off-line small-step electromagnetic transient simulation are inefficient due to the tremendous computational burden of the MMC-HVDC [9].

At present, real-time electromagnetic transient simulation is dependent on high-performance processors and efficient hardware architecture, such as the multi-core central processing unit (CPU), field programmable gate arrays (FPGAs), or heterogeneous CPU-FPGA. Real-time simulation technology is necessary to more effectively solve engineering problems [10].

The circuit parameters of the high-voltage large-capacity MMC-HVDC transmission system change dynamically with

the number of inserted sub-modules (SMs), resulting in a time-varying network matrix. This matrix significantly increases the difficulty of obtaining real-time solutions for the system. At present, the network partition algorithm is an important technology used to realise real-time solutions for high-dimensional time-varying networks [11].

The purpose of network partition is to realise the decoupling of large-scale systems, so that all decoupled subsystems can be calculated in parallel. There are currently three methods used to achieve network partition: Transmission line decoupling [12], latency decoupling [13], and the multi-area Thevenin equivalent (MATE) method [14].

The transmission line decoupling method realises the natural decoupling of the network at both ends of the transmission line based on its travelling wave characteristics. This method has high simulation accuracy but can only be applied when the travel time of the transmission line is greater than the simulation step. The decoupling point must have a transmission line with sufficient length, which limits its applicability [15].

Latency decoupling works by manually introducing a delay factor. Latency decoupling can be performed by waveform relaxation (WR) [16] or the latency insertion method [17]. Waveform relaxation introduces relaxation to the variables, which can distort the results or cause numerical instability in the direct solution. Generally, within each simulation step, it is necessary to obtain the real result through multiple iterations. Various techniques have been proposed to improve convergence [18–20]; however, the iterative process increases the computational burden which is contrary to the purpose of network partition.

Latency insertion method uses the specific structures of the inductor and capacitor to realise the latency decoupling of the node voltage and branch current based on an explicit integration algorithm [21, 22]. However, this algorithm has poor numerical stability. The leap-frog method, a semi-implicit integration algorithm with second-order accuracy, can be used to reduce the risk of numerical instability [23]. The latency insertion method application requires a certain topology and introduces latency between the node voltage and branch current, which has a certain impact on simulation accuracy.

The MATE method is based on the network equation wherein the node voltage or branch current is a correlation variable. Gauss elimination is applied to decouple the network equation into a correlation variable equation and two sub-net network equations, thus realising the parallel computing of the two subnets [24]. The computing efficiency of MATE is related to the selection of the correlation variables, the number of subnets, and the size of the correlation network. Therefore, it is necessary to select the decoupling point carefully when considering computing efficiency, even if the method can achieve decoupling anywhere and has no calculation error [25].

On the basis of network partition, multi-rate simulation technology can improve computing efficiency and reduce resource consumption. It is generally understood that multi-rate simulation technologies require small-step simulation for power electronic devices with fast dynamics (e.g., MMC) and large-step simulation for traditional alternating current (AC) systems, which have slow dynamics [26]. The data interaction of multi-rate simulation affects the simulation accuracy and calculation stability, especially regarding the high-frequency characteristics of the system.

At present, the real-time simulation of MMC-HVDC is mainly based on the above network partition algorithms. Taking the commercial real-time simulation platforms as examples, an advanced digital power system simulator (ADPSS) uses the transmission line decoupling method to achieve the decoupling between AC and direct current (DC) systems [15]. However, there are limitations that cannot be applied when there are no transmission lines or the length of the transmission lines is not long enough. In response to this situation, ADPSS proposes an equivalent transmission line decoupling method, which utilises the leakage inductor of the converter transformer and constructs an equivalent transmission line through a parallel capacitor [27]. However, it will affect the simulation accuracy of MMC high-frequency characteristics, especially in the multi-rate simulation, as the travel time of the equivalent transmission line needs to be greater than the large step. Real time digital simulator (RTDS) utilises an interface transformer model to achieve decoupling of large-step and small-step networks, which is essentially a type of the latency decoupling method [28]. It achieves decoupling between AC and DC systems by introducing delay between the primary-side current and the secondary-side voltage of the converter transformer. As the ratio of large step to small step increases, the simulation errors caused by delay increases, and the impact on the simulation accuracy of MMC high-frequency characteristics becomes greater. In addition, the interface transformer may cause the numerical instability, and the damper branches are usually required to be connected on the primary side of the transformer, which will have a significant impact on the analysis of high-frequency resonance for MMC-HVDC. Real time laboratory (RTLAB) uses the state–space method to calculate the valve model of MMC within a small step, and the node-voltage method to solve the entire network within a large step, so that the time-varying network equation caused by the dynamical change of the number of inserted SMs can be solved within a large step [29]. However, the interaction between valves is flawed because it only happens once per large step. It is our belief that the correct approach is to model the entire converter with a small step so that the high-frequency characteristics of MMC can be correctly represented [30].

The most basic principle of data interaction between large-step and small-step networks is the average principle [31, 32]. When calculating large-step variables, the average of small-step variables is used. When calculating small-step variables, the interpolation of large-step variables is used. Although all the solution results of the small-step variables within a large step are fully used to solve the large-step variables, which can help to improve the numerical stability, the simulation errors gradually increase with the increase of frequency.

Due to the late discovery of the high-frequency resonance of MMC-HVDC, the current real-time simulation technologies of MMC-HVDC have not fully considered the simulation

accuracy for the high-frequency characteristics of MMC. As the stability problems of the power system gradually develop towards the high-frequency range, it is necessary to improve the simulation accuracy of the high-frequency characteristics of the system in real-time simulation.

A parallel multi-rate scheme with an accurate high-frequency characteristic simulation capability for the MMC-HVDC was developed in the present study. We used a novel converter transformer decoupling method and multi-rate data interaction mode. A real-time parallel multi-rate electromagnetic transient simulation platform was constructed for the MMC-HVDC based on the FPGA array. We analysed critical factors affecting the simulation accuracy of high-frequency MMC characteristics. We also compared the real-time simulation results for the developed simulation platform with off-line simulation results for the power systems computer aided design/electromagnetic transient including DC (EMTDC) (PSCAD/EMTDC) and real-time simulation results for the RTDS platform to prove the effectiveness of the proposed method.

## 2 | PARALLEL MULTI-RATE SIMULATION SCHEME FOR MMC-HVDC

### 2.1 | Overall scheme

To reflect the scale of the system without losing generality, we use the four-terminal true bipolar MMC-HVDC as the target system here. Its topology is shown in Figure 1. The four converters are all half-bridge MMC in which each arm contains $N$ half-bridge SMs. The DC ports of adjacent converters are interconnected through a smoothing reactor and transmission line to form a four-terminal loop network.

The parallel multi-rate simulation scheme proposed in this paper is shown in Figure 2, where ①, ②, and ③ are network partition positions. ① uses a DC transmission line to achieve decoupling between converters, ② uses a converter transformer to achieve decoupling between the converter and AC system, and ③ uses the arm reactor to achieve decoupling within the converter. ④ and ⑤ are the data transmission channels; ④ is the data exchange between large-step and small-step systems using the converter transformer as the multi-rate interface and ⑤ is the data exchange between the converter and control system.

We selected network partition positions with the goal of achieving uniform network partition and accurate real-time simulation. Due to the consistent topology and equivalent dimensions of each converter, the selected position ① to achieve uniform network partition and optimise the allocation of computing resources. To satisfy the simulation accuracy requirements of the DC system and reduce the computational complexity of the AC system, we also conducted multi-rate simulation of the AC/DC system. The network partition position ②, that is, the converter transformer, was used as the decoupling point of the AC/DC system, that is, the multi-rate simulation interface. This limits the small-step system to a small scale and reduces the computational burden.

Due to the presence of multiple arms with dynamic changes in equivalent parameters within the DC system, it is difficult to conduct real-time calculations across the small-step system. We used ③, that is, the arm reactor, to further divide the time-varying parameter branches of the small-step system into a single node subsystem for enhanced efficiency.

The establishment of data transmission channels achieves data exchange between systems at different rates. In the target shown in Figure 2, the multi-rate system includes a large-step simulation system on the AC side, a small-step simulation system on the DC side, and an MMC control system. Data-exchange delay between different rate systems significantly affects high-frequency characteristic simulation accuracy. To remedy this, we established a data transmission channel ④ between large-step and small-step systems and a data transmission channel ⑤ between the control system and the primary system to improve the simulation accuracy of frequency characteristics.

① and ③ use relatively sophisticated transmission line decoupling technology and travelling-wave characteristics of the transmission line to achieve natural decoupling of the systems on either side of that line, which ensure accurate simulations. Due to the small-step simulation at ①, the length of the DC transmission line readily satisfies the conditions for

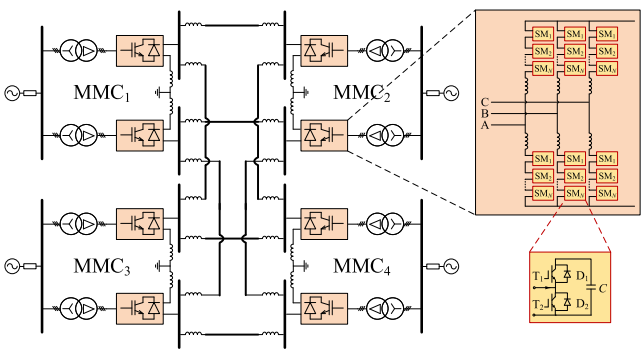


**FIGURE 1** Modular multilevel converter-based high-voltage direct current (MMC-HVDC) topology.

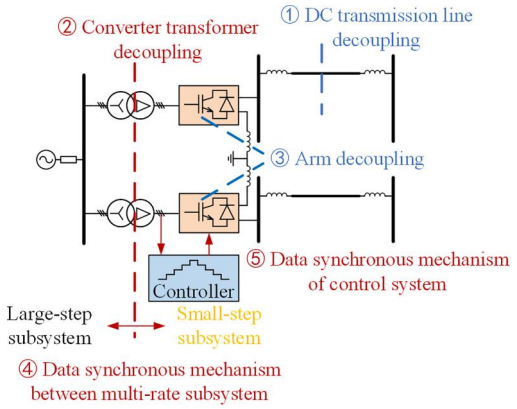


**FIGURE 2** Target scheme for the proposed parallel multi-rate simulation method.

transmission line decoupling. Even in the back-to-back connection mode, the equivalent transmission line can be formed based on the smoothing reactor or by adding a small series reactor and parallel capacitor. Accuracy is thus not markedly affected in the small-step simulation. Similarly, ③ constructs an equivalent transmission line based on the arm reactor by adding a ground capacitor for the arm decoupling of the converter. Due to the large value of the arm reactor, which ranges from tens to hundreds of mH, the additional capacitor is very small in the small-step simulation, has a very small value —smaller than nF—and has very little impact on the system's high-frequency characteristics.

② is the key node connecting the large-step and small-step simulation systems. The choice of the decoupling method significantly affects the accuracy of MMC frequency characteristic simulations. Existing commercial real-time simulation platforms generally use transmission line decoupling or WR to achieve decoupling between AC and DC systems. The former is based on the leakage inductance of the converter transformer and builds the equivalent transmission line by adding ground capacitance [33]. In accordance with the simulation step of the large-step system, the value of the additional capacitance is relatively large and significantly affects the accuracy of high-frequency MMC characteristic simulations. The latter achieves decoupling between the systems on both sides of the converter transformer by introducing a delay factor between the primary and secondary sides, but this approach significantly impacts numerical stability and simulation accuracy.

In this study, we used the Gauss elimination method to decouple primary and secondary sides of the converter transformer, based on the characteristics of the gyrator and variables in the hybrid equation. This allows for error-free decoupling between AC and DC systems without increasing the network dimensions. The computational efficiency of the proposed converter transformer decoupling model is affected by the states of the subsystems on both sides. Efficiency is significantly reduced when there are time-varying parameters in the subsystems.

The AC-side system is usually composed of linear components, and the node admittance matrix is constant when the topology remains unchanged. Even if the topology changes under conditions such as faults, the inverse matrix of the node admittance matrix under various topologies can be stored in the preprocessing process prior to the simulation to prevent matrix inversion from decreasing simulation efficiency. In addition, the decoupling effect of transmission lines and transformers in the AC system reduces the dimensionality of the AC-side system connected to the converter transformer, thereby reducing the computational burden of the converter transformer decoupling system.

There are numerous SMs in the arm of the DC-side system, and the number of on-state SMs dynamically changes. The use of the Thevenin equivalent model based on the trapezoidal integration method in the arm can ensure accurate frequency characteristic simulations with strong numerical stability.

The above factors create a non-linear trend in the equivalent parameters of the arm, which seriously limit the calculation speed. Due to the arm decoupling effect of ③ in the proposed simulation scheme, the DC-side system connected to the converter transformer is a fixed-admittance Thevenin branch which improves the computational efficiency of the converter transformer decoupling system.

The network partition strategy proposed in this paper, which combines ①, ②, and ③, can achieve parallel real-time simulation of the MMC-HVDC while ensuring an accurate simulation of high-frequency MMC characteristics. This strikes an effective balance between efficiency and accuracy.

④ is the data transmission channel for the systems on both sides of ③, which is the key link in achieving multi-rate simulation. The data transmission process from the small-step system to the large-step system is the key factor in simulation accuracy. The small-step system has a rapid update speed, which completes multiple calculations between two adjacent large-step simulation times during which time its topology may change. All calculation results of the small-step system between large-step simulation times are generally considered comprehensively in multi-rate simulation processes, where the average value is used as interactive data. However, the frequency-dependent characteristics of the MMC are a direct embodiment of the dynamic changes in topology. Average values in the multi-rate simulation of MMC-HVDC thus significantly impact the simulation accuracy of high-frequency MMC characteristics. We developed a data synchronous interaction mechanism for the multi-rate simulation system, which improves this simulation accuracy through the interaction of synchronous values.

⑤ is an important part of the real-time digital simulation process, as it conducts data exchange between the control system and the primary system. During off-line simulation, the control system is serially calculated with the primary system. The simulation step is consistent with the control cycle, and there is no asynchronous data interaction. In practice, the primary system operates continuously and the sampling, calculation and triggering of the control system are not dependent on its timing. There is no asynchronous data interaction in the control system either. During real-time simulation, the primary system and control system are calculated in parallel; the simulation step of the primary system is inconsistent with the control cycle. It is also necessary to consider the impact of control link delay in the actual controller on the high-frequency characteristics of the MMC. We propose a data synchronous interaction mechanism between the digital simulator and the digital controller to simulate the link delay for accurate high-frequency MMC characteristic simulation.

We established a multi-rate simulation system based on data transmission channels ④ and ⑤ with full consideration of the differences in the high-frequency MMC characteristics caused by delayed data interaction between multi-rate digital systems. This scheme improves the frequency characteristic simulation accuracy of the system. The transmission line decoupling technology used by ① and ② is relatively

sophisticated, so we do not discuss it in detail here. The specific implementation process of ③, ④, and ⑤ is explained in detail below.

## 2.2 | Converter transformer decoupling method

Figure 3 shows the YNd11 connection set of the converter transformer in Figure 1. We use this setup as an example to demonstrate the process of decoupling of AC and DC sides of the system. The derivation process is similar for other connection sets.

$v_{1A}$, $v_{1B}$, and $v_{1C}$ represent the three-phase voltages at the primary side of the converter transformer. $v_{2A}$, $v_{2B}$, and $v_{2C}$ represent the three-phase voltages at the secondary side of the converter transformer. $L_T$ represents the leakage inductance of the converter transformer with reference to the secondary side, and $R_T$ represents the equivalent resistance of eddy current loss of the converter transformer with reference to the secondary side.

We set $\boldsymbol{V_{ac}} = [v_{1A}, v_{1B}, v_{1C}, \ldots]^T$ as the node voltage vector of the AC side and $\boldsymbol{V_{dc}} = [v_{2A}, v_{2B}, v_{2C}, \ldots]^T$ as the node voltage vector of the DC side. $\boldsymbol{I_{ac}}$ is the node injection current vector of the AC side, $\boldsymbol{I_{dc}}$ is the node injection current vector of the DC side, and $\boldsymbol{I_T} = [i_{2A}, i_{2B}, i_{2C}]^T$ is the secondary-side current vector of the converter transformer. The hybrid analysis method can be applied to obtain the network equation of the transformer:

$$\begin{bmatrix} \boldsymbol{Y_{11}} & \boldsymbol{0} & \boldsymbol{M_{13}} \\ \boldsymbol{0} & \boldsymbol{Y_{22}} & \boldsymbol{M_{23}} \\ \boldsymbol{M_{31}} & \boldsymbol{M_{32}} & \dfrac{2L_T}{\Delta t}\boldsymbol{E} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_{ac}} \\ \boldsymbol{V_{dc}} \\ \boldsymbol{I_T} \end{bmatrix} = \begin{bmatrix} \boldsymbol{I_{ac}} \\ \boldsymbol{I_{dc}} \\ -\boldsymbol{V_{LH}} \end{bmatrix} \tag{1}$$

where $\boldsymbol{E}$ is the identity matrix, $\Delta t$ is the simulation step of the DC side, $\boldsymbol{Y_{11}}$ and $\boldsymbol{Y_{22}}$ are the node admittance matrices of the AC-side system and the DC-side system, respectively, $\boldsymbol{M_{13}}$ and $\boldsymbol{M_{31}}$ are the interconnected matrices between the AC-side system and the converter transformer, respectively, $\boldsymbol{M_{23}}$ and $\boldsymbol{M_{32}}$ are the interconnected matrices between the DC-side system and the converter transformer, respectively, and $\boldsymbol{M_{13}}$, $\boldsymbol{M_{31}}$, $\boldsymbol{M_{23}}$, and $\boldsymbol{M_{32}}$ are as shown in Equation (2). $\boldsymbol{V_{LH}}$ is the voltage source of the differential model of the leakage inductance. Taking phase A as an example, $v_{LHA}$ is shown in Equation (3).

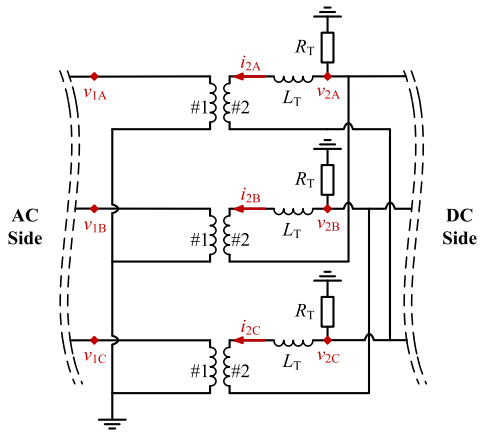


**FIGURE 3** Converter transformer topology.

$$\begin{cases} \boldsymbol{M_{13}} = \begin{bmatrix} \mathrm{diag}\left(-\dfrac{1}{n}, -\dfrac{1}{n}, -\dfrac{1}{n}\right) \\ \boldsymbol{0}_{(N_{ac}-3)\times 3} \end{bmatrix}_{N_{ac}\times 3} \\ \boldsymbol{M_{31}} = \begin{bmatrix} \mathrm{diag}\left(\dfrac{1}{n}, \dfrac{1}{n}, \dfrac{1}{n}\right) & \boldsymbol{0}_{3\times(N_{ac}-3)} \end{bmatrix}_{3\times N_{ac}} \\ \boldsymbol{M_{23}} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \\ \boldsymbol{0}_{(N_{dc}-3)\times 3} \end{bmatrix}_{N_{dc}\times 3} \\ \boldsymbol{M_{32}} = \begin{bmatrix} -1 & 0 & 1 & \\ 1 & -1 & 0 & \boldsymbol{0}_{3\times(N_{dc}-3)} \\ 0 & 1 & -1 & \end{bmatrix}_{3\times N_{dc}} \end{cases} \tag{2}$$

where $n$ is the ratio of the converter transformer, $N_{ac}$ is the node number of the AC-side system, and $N_{dc}$ is the node number of the DC-side system.

$$v_{LHA}(t) = -i_{2A}(t-\Delta t)\frac{4L_T}{\Delta t} - v_{LHA}(t-\Delta t) \tag{3}$$

We can take $\boldsymbol{I_T}$ as a correlation variable and apply the Gauss elimination method to Equation (1) to eliminate $\boldsymbol{V_{ac}}$ and $\boldsymbol{V_{dc}}$ so that the equation of the correlation network is

$$\begin{aligned} &\left(\frac{2L_T}{\Delta t}\boldsymbol{E} - \boldsymbol{M_{31}}\boldsymbol{Y_{11}^{-1}}\boldsymbol{M_{13}} - \boldsymbol{M_{32}}\boldsymbol{Y_{22}^{-1}}\boldsymbol{M_{23}}\right)\boldsymbol{I_T} \\ &= -\boldsymbol{V_{LH}} - \boldsymbol{M_{31}}\boldsymbol{Y_{11}^{-1}}\boldsymbol{I_{ac}} - \boldsymbol{M_{32}}\boldsymbol{Y_{22}^{-1}}\boldsymbol{I_{dc}} \end{aligned} \tag{4}$$

After solving the correlation network and obtaining the correlation variable $\boldsymbol{I_T}$, the node voltage of each subnet can be solved in parallel as follows:

$$\begin{cases} \boldsymbol{Y_{11}}\boldsymbol{V_{ac}} = \boldsymbol{I_{ac}} - \boldsymbol{M_{13}}\boldsymbol{I_T} \\ \boldsymbol{Y_{22}}\boldsymbol{V_{dc}} = \boldsymbol{I_{dc}} - \boldsymbol{M_{23}}\boldsymbol{I_T} \end{cases} \tag{5}$$

The correlation variable for the converter with true bipolar topology is the secondary-side currents of the converter transformers in the positive and negative converter. This derivation is similar to be above, so we do not repeat it here.

## 2.3 | Data synchronisation mechanism between multi-rate subsystems

The correlation network provides correlation variables for the subsystems of the converter transformer decoupling system. The solution of the correlation network depends on the node injection current provided by the subsystems. Therefore, in the multi-rate simulation process, the correlation network serves as the data channel for the large-step and small-step subsystems. The simulation step of the correlation network is consistent with that of the small-step subsystem, that is, the DC-side subsystem; the update rate of the large-step subsystem, that is, the AC-side subsystem, is slow. Define the small step as $\Delta t$, the large step as $\Delta T$, the time of the simultaneous solution of subsystems as synchronous time, and the time of the separate solution of DC-side subsystem between two adjacent synchronous times as asynchronous time.

At the asynchronous time, the linear interpolation of the node injection current of the AC-side subsystem of the adjacent two synchronous times is usually used as the input of the correlation network. The output result is used for the DC-side subsystem solution.

At the synchronous time, the influence of multiple calculations of the small-step subsystem on the large-step subsystem is typically taken into account. The mean value of correlation variables at all times between two adjacent synchronous times is used as the input of the large-step subsystem. However, this introduces delay. The trend of the mean value lags behind the synchronous value, which ultimately creates phase deviation in the high-frequency impedance characteristics of the MMC. The phase-frequency curve moves in the low-frequency direction, where phase deviation increases as frequency increases.

To ensure accurate high-frequency characteristic simulation, in this paper, we propose using the synchronous value of the AC-side and DC-side subsystems for data interaction at the synchronous time (Figure 4), where $t_1$ and $t_2$ are two adjacent synchronous times.

## 2.4 | Data synchronisation mechanism for control system

The sampling, station control, valve control, protection, and other links in the MMC-HVDC control system are independent of each other, resulting in fairly lengthy delay in the control link. To ensure the accuracy of the MMC-HVDC high-frequency characteristics, it is necessary to consider the effect of delay in the control system. In the simulation, the delay is usually manually added to the trigger pulse generation link. In addition, the sampling frequency of the MMC controller in an actual project is limited. Generally, the control cycle is much larger than the simulation step of the DC-side subsystem. For an effective simulation, the control system and primary system need to be synchronised. We define the sampling time of the control system as the synchronous time. The data interaction principle between the control system and the primary system is shown in Figure 5.

The data interaction process is as follows.

(1) When $t = t_1$, the control system collects the three-phase voltage, three-phase current, arm current, and other signals of the primary system as its inputs.
(2) When $t = t_2$, the control system completes a control cycle, generates the trigger pulses, and sends them to the delay link. At the same time, it collects the signals of the primary system to enter the next control cycle.
(3) After the trigger pulses are delayed for $T_d$, they are sent to the primary system as the trigger pulses of the next control cycle.

# 3 | HARDWARE IMPLEMENTATION

The FPGA is a semi-custom circuit used in the application specific integrated circuit, which is a programmable logic array. Unlike the CPU, the FPGA has parallel architecture, extremely fast calculation speed, and better capability for processing local and repetitive work, which is suitable for the calculation of the MMC-HVDC. We used the Xilinx VC707 development kit as the hardware carrier to operate the parallel multi-rate simulation scheme described above, develop the primary system solver and MMC controller of the four-terminal true bipolar MMC-HVDC, and establish a real-time simulation platform based on the FPGA array.

## 3.1 | Primary system solver based on FPGA

The solution of the primary system is divided into two steps, the first is valve calculation and the second is circuit calculation. The former generates the Thevenin equivalent circuit of the arm according to the trigger signals of SMs, the capacitor

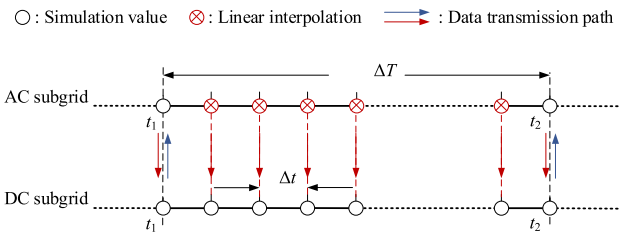


**FIGURE 4** Data interaction principle of multi-rate subsystems.

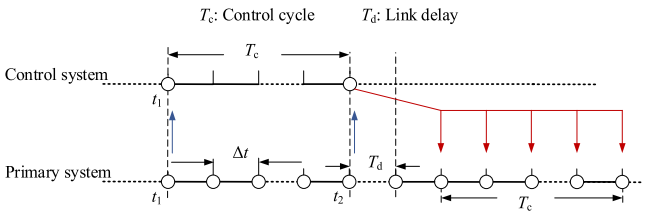


**FIGURE 5** Data interaction principle of the control system.

voltages of SMs and the current of the arm, and the latter solves the network equation of the system including the equivalent model of the arm.

We developed the valve calculation module based on the pipelining technique by incorporating the unique advantages of the FPGA's parallel computing architecture. For an MMC with no more than 256 SMs on a single arm, $N = 256$ is taken as the total number of SMs on the single arm to adapt to the change in the number of SMs. We used this parameter and set four pipelines for parallel computing. Each pipeline is mainly used to update the capacitor voltage of 64 SMs and the equivalent calculation of the voltage of this part of the arm. In the pipeline, the data stream of the SMs' capacitor voltage is updated and summed. Each pipeline operates synchronously, which accelerates the data processing rate.

To further optimise hardware resources and ensure accuracy, we used a 64-bit fixed-point number in the valve calculation module considering the fast rate and low Look Up Table consumption of fixed-point calculation. This includes 32 bits in the integer part and 32 bits in the decimal part. At the input and output ports of the valve calculation module, an Intelletual Property Core (IP Core) is used to convert number between floating-point number and fixed-point number.

In the circuit calculation module, the single-terminal converter can be decoupled into five subsystems based on the proposed parallel multi-rate simulation scheme. We named them according to their respective function and location as the positive DC subsystem, the negative DC subsystem, the grounded DC subsystem, the AC subsystem of the multi-rate subsystem, and the DC subsystem of the multi-rate subsystem. Considering the solution of the correlation layer of the multi-rate subsystem, we divided the circuit calculation module into six units: the positive DC subsystem module, negative DC subsystem module, grounded DC subsystem module, correlation layer of the multi-rate subsystem module, AC subsystem of the multi-rate subsystem module, and DC subsystem of the multi-rate subsystem module.

The circuit calculation module bears a large computational burden and consumes an excess of Digital Signal Processing resources in the process of fixed-point calculation, which makes it impossible to integrate the calculation of an entire converter on the same development kit. Therefore, we used the floating-point number for the circuit calculation module. Vivado, the integrated design environment of the FPGA, provides the IP core for four arithmetic operations of the floating-point number. This is a better use of resources, but excessive use still leads to a high level of resource consumption.

The function of the circuit calculation module is to solve the node voltage equation. Despite a greatly reduced number of nodes and branches in our decoupled subsystem, the calculation method still significantly impacts resource usage and timing. To optimise the resource usage, we reused the logic to solve the node voltage equation. Each circuit calculation module was configured with a fixed number of IP cores for floating-point calculation.

First, we derived the expression of each variable according to the network equation and determined the number and order of the four arithmetic operations based on the equation transformation. The current calculation progress was judged by adding counters at the input and output ports of the IP core. The valid signal of the data was taken as the flag; then, existing variables and intermediate variables were input to the IP core in the form of a data flow according to the flag and the counter at the input port. With the counter at the output port as the flag, we assigned the output of the IP core to the intermediate variable to form logic reuse.

For the purposes of computing efficiency, the add operation, subtract operation, multiply operation, and divide operation are performed in parallel. Their respective outputs can be inserted into the input data flow of the corresponding IP core as required, thus effectively reducing interruptions to the data flow caused by the inherent computing time of the IP core and markedly enhancing the computing efficiency.

Based on the above design, we integrated the primary system solution of the single-terminal true bipolar MMC with no more than 256 SMs of a single arm into one FPGA development kit. The overall framework and calculation logic are shown in Figure 6. The converter at each terminal realises high-speed transmission of the transmission line decoupling signals between FPGA arrays through the Aurora interface, which has a communication rate of 2 Gbps, meeting the requirements for small-step real-time simulation.

## 3.2 | MMC controller based on FPGA

Considering that the computational logic of the control system is relatively simple, we can use fixed-point calculation to realise the functions of the control system. Figure 7 shows the overall architecture of our MMC controller. The controller integrates positive pole and negative pole control systems of the single-terminal true bipolar MMC, which have the same control logic, including a phase lock loop, Park transformation, outer

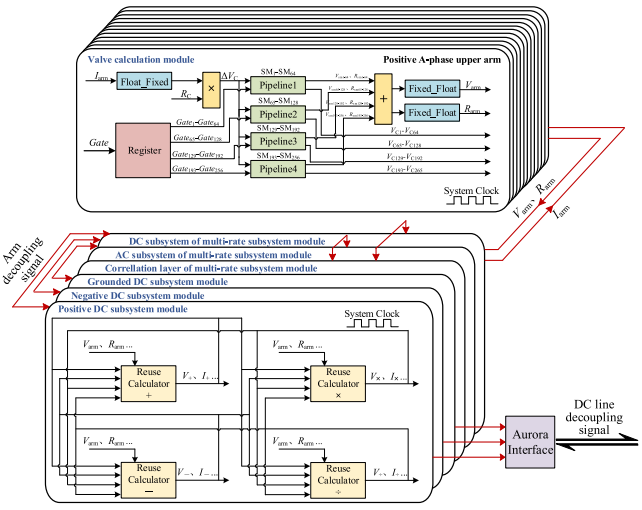


**FIGURE 6** Primary system solver based on field programmable gate array (FPGA).

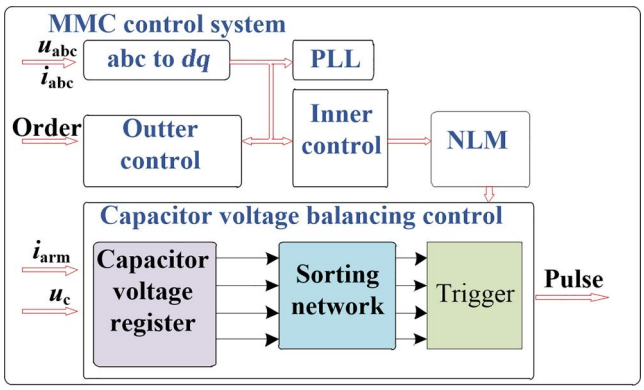


**FIGURE 7** Modular multilevel converter (MMC) controller based on field programmable gate array (FPGA).

control, inner control, nearest level modulation, and capacitor voltage balancing control.

The controller receives AC voltage and current signals, arm current signals, and SM capacitor voltage signals from the primary system solver, then sends the SMs' trigger signals to the primary system solver. We integrated the primary system and control system of a single-terminal true bipolar MMC on the same FPGA development kit for resource optimisation and allocation. The controller and the primary system solver are connected through programmable internal connection resources without communication delay. When the controller and the primary system solver need to be separated, they can complete data interaction based on Aurora.

To fully exploit the parallel computing advantages of the FPGA, each control module was designed in parallel. Control modules that are independent of each other or have the same function can be executed in parallel to minimise the computing time of the control system. For the capacitor voltage sort, which has the greatest impact on the resource consumption and time performance of the controller, we adopted the bitonic sorting algorithm. It is suitable for the FPGA and can be implemented in parallel. The number of input channels in the sorting network is consistent with the number of pipelines in the valve calculation module. Due to the high resource consumption and the long computing time of the sorting network, considering resource allocation and timing optimisation issues, the sorting module was multiplexed by triggering the capacitor voltage memories of the six arms in turn and sending them to the same capacitor voltage sorting network. As per the performance requirements of the sorting module, we also controlled at least 4 system clocks between the capacitor voltage data flows of the two arms, as shown in Figure 7.

### 3.3 | Resource consumption and time performance of FPGA

We built a real-time simulation platform of a four-terminal true bipolar MMC-HVDC based on the FPGA array, as shown in Figure 8. Four FPGA development kits were used as the

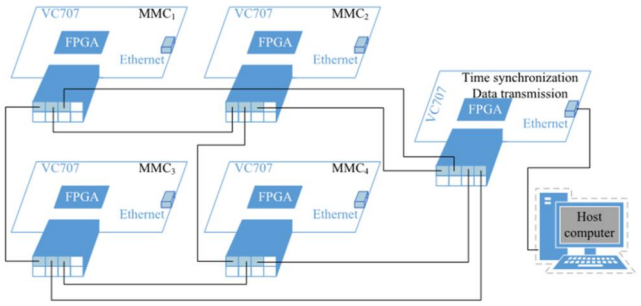


**FIGURE 8** Real-time simulation platform based on field programmable gate array (FPGA).

simulators for four converters. One FPGA development kit was used as a time synchronisation device to transmit synchronisation signals to the four simulators, while receiving the data required to be displayed from the four converters and transmitting them to a host computer via Ethernet protocol.

The frequency of the system clock was set to 100 MHz. The resource consumption and temporal performance of the real-time simulator of the single-terminal MMC are shown in Table 1. The computing time of primary system is within 2 μs, and the control cycle of MMC controller is within 10 μs, meeting the requirements for small-step real-time simulation.

## 4 | FACTORS AFFECTING HIGH-FREQUENCY CHARACTERISTIC SIMULATION ACCURACY

The positive sequence high-frequency impedance characteristics of the AC side of the MMC are mainly affected by the leakage inductance of the converter transformer, the inductance of the arm, the control link delay $T_d$, and the inner control. The impedance-frequency relationship can be approximately expressed as follows [34]:

$$Z_{MMC}(s) = \frac{sL + G_{delay}(s)G_{PI}(s)}{1 - G_{delay}(s)} \tag{6}$$

where $L = L_T + L_{arm}/2$, $G_{PI}(s)$ is the proportional integral control, $G_{delay}(s) = e^{-sT}$ is the equivalent delay link, and $T$ is the equivalent delay.

Previous studies have tended to focus on the pseudo bipolar MMC-HVDC. The primary and secondary sides of the converter transformer have a stelliform connection, so the equivalent delay $T = T_d$.

We considered the influence of different connection sets of converter transformers in modifying the equivalent delay. In the YNd11 connection set shown in Figure 3, for example, the modified $G_{delay}(s)$ is shown as Equation (7) where the secondary side leads the primary side by $\pi/6$ rad:

$$G_{delay}(s) = e^{-s\left(\frac{\pi}{6\omega}+T_d\right)} \tag{7}$$

## 4.1 | Influence of simulation step on accuracy

In our simulation process, the inductance and capacitance are solved by the implicit trapezoidal integration method. Although the method yields high accuracy, it is still an approximate solution method which will have some errors.

The difference equation of inductance $L$ derived by the implicit trapezoidal integration method and the difference equation of the unit-length short-circuit lossless transmission line with $Z_c = 2\ L/\Delta t$, $\tau = \Delta t/2$ are completely consistent, where $Z_c$ and $\tau$ are the characteristic impedance and time constant of the transmission line, respectively [35]. For a short-circuit lossless transmission line with these parameters, the input impedance can be calculated as follows:

$$Z_{\text{input}} = \mathrm{j} Z_c \tan(\beta l) \tag{8}$$

where $\beta = \omega\tau/l = \omega\Delta t/2$ represents the phase constant. Equation (8) can be reformulated to determine the input impedance as follows:

$$Z_{\text{input}} = \mathrm{j}\omega L \frac{\tan\left(\omega \frac{\Delta t}{2}\right)}{\omega \frac{\Delta t}{2}} \tag{9}$$

According to the equivalence relation, the impedance of inductance $L$ solved by the implicit trapezoidal integration method is consistent with Equation (9), which has amplitude deviation from the actual impedance of inductance $L$ at $\mathrm{j}\omega L$. This deviation increases monotonously with the frequency and simulation steps.

By modifying the error according to Equation (9), the high-frequency impedance of the AC side of the MMC in the multi-rate simulation is as follows:

$$Z_{\text{MMC}}(s) = \frac{sL \frac{\tan\left(\omega \frac{\Delta T}{2}\right)}{\omega \frac{\Delta T}{2}} + G_{\text{delay}}(s) G_{\text{PI}}(s)}{1 - G_{\text{delay}}(s)} \tag{10}$$

The differential item in the denominator of Equation (10) determines the amplitude of MMC impedance at higher frequencies, which is affected by the error of the implicit trapezoidal integration algorithm. The simulation error of high-frequency impedance under $f = 3000$ Hz and $\Delta T = 50$ μs is about 8%, which has little influence on the high-frequency resonance results.

**TABLE 1** Resource consumption and temporal performance of field programmable gate array (FPGA).

| | Resource consumption (%) | | | | Temporal performance | |
|---|---|---|---|---|---|---|
| Module | LUT | Register | BRAM | DSP | Clock | Time (μs) |
| 1 | 11.90 | 5.64 | 4.66 | 17.57 | 80 | 0.80 |
| 2 | 2.83 | 1.02 | 0.15 | 0.21 | 81 | 0.81 |
| 3 | 2.90 | 1.02 | 0.15 | 0.21 | 81 | 0.81 |
| 4 | 4.36 | 1.79 | 0.30 | 0.24 | 89 | 0.89 |
| 5 | 4.71 | 2.69 | 0 | 0.21 | 82 | 0.82 |
| 6 | 8.46 | 4.13 | 17.09 | 0 | 821 | 8.21 |
| 7 | 3.97 | 1.73 | 0 | 6.54 | 116 | 1.16 |
| 8 | 1.18 | 0.53 | 0 | 12.79 | 7 | 0.07 |
| 9 | 0.62 | 0.26 | 0 | 4.72 | 9 | 0.09 |
| 10 | 0.53 | 0.24 | 0 | 3.79 | 8 | 0.08 |
| 11 | 0.64 | 0.19 | 0 | 5.14 | 4 | 0.04 |
| 12 | 15.45 | 6.61 | 0 | 65.93 | 144 | 1.44 |
| Total | 50.61 | 22.90 | 22.35 | 84.37 | —— | —— |

*Note*: 1: Valve calculation module (12 arms). 2: Positive DC subsystem module. 3: Negative DC subsystem module. 4: Grounded DC subsystem module. 5: Multi-rate subsystem module. 6: Capacitor voltage balancing control module (double poles). 7: Phase lock loop (single pole). 8: Park transformation (single pole). 9: Outer control (single pole). 10: Inner control (single pole). 11: Nearest level modulation (single pole). 12: Total control module (double poles, except voltage balancing control).

Abbreviations: DSP, digital signal processing; LUT, look up table.

## 4.2 | Influence of alternating current network on accuracy

For the converter transformer decoupling system, the interpolation of the node injection current of the large-step subsystem is necessary to obtain the input that solves the system at the asynchronous time. The error of the linear interpolation increases as the frequency of the injection current increases.

We established a simple multi-rate simulation model (Figure 9) to analyse the influence of the AC network on the accuracy of simulated high-frequency characteristics of the DC system.

$v_s$ is the sinusoidal voltage source, $Z$ is the network impedance of the large-step side, $L$ is the inductance of the small-step side, and $v_1$ and $v_2$ are the voltages of node 1 and node 2, respectively. With the inductance between node 1 and node 2 as the interface of the large-step and small-step networks, the multi-rate simulation of the circuit can be realised based on the method discussed in Section 2.

When $Z$ is resistive, we set $Z = 4\ L/\Delta T$, $\Delta T = 2\Delta t$, and the cycle of $v_s$ as $8\Delta T$. Under these conditions, the equivalent node injection current of the large-step side is $i_e(t) = v_s(t)/Z$. Figure 10(a) shows the value of $i_e$, which is used as the input of the correlation network at the synchronous and asynchronous times. The red circle in the figure marks the linear interpolation at the asynchronous time. Because $i_e$ is not affected by the simulation results, the error introduced in the small-step network is only caused by the interpolation algorithm. The solution of the multi-rate simulation is consistent with the solution of the small-step simulation with the node injection current, as shown in Figure 10(b). When the large-step

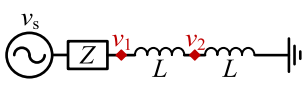


**FIGURE 9** Simple multi-rate circuit.

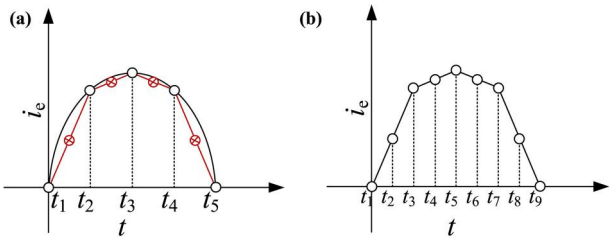


**FIGURE 10** Equivalent node injection current: (a) Multi-rate simulation; (b) Small-step simulation.

network is resistive, the small-step network shows no error regarding the accuracy of high-frequency characteristics.

When $Z$ is inductive, the solution of the small-step network at the asynchronous time cannot be fed back to the equivalent source of the inductive element of the large-step network, which reduces the accuracy of high-frequency characteristics. Taking the circuit shown in Figure 9 as an example, we set $Z = \mathrm{j}2\omega L$, $\Delta T = 2\Delta t$, and the initial state as 0 when $t = 0$. Based on these conditions, the voltage of node 1 when $t = \Delta T$ is $v_1\ (\Delta T) = 5v_s\ (\Delta T)/9$. However, in the actual system, the voltage of impedance $Z$ and the voltage of inductance on the right of node 1 should be equal. Therefore, as per the large-step side of the multi-rate simulation system, the characteristics of the components on the right of node 1 change; that is, there is an error in the high-frequency characteristics of the small-step network.

To sum up, when the large-step network contains inductive, capacitive or controlled elements, the impedance-frequency characteristics of the port impedance at the multi-rate interface of the large-step network have errors compared with the real impedance-frequency characteristics of the small-step network.

## 5 | SIMULATION VALIDATION

To test the performance of the developed multi-rate real-time simulator, we conducted control experiment in PSCAD/EMTDC and RTDS respectively in which the simulation step of PSCAD/EMTDC is 2 μs and the simulation step of RTDS is 50 μs/2 μs. It is generally believed that the simulation accuracy of PSCAD/EMTDC with small step is higher than that of real-time simulation. Therefore, this section believes that the smaller the error between the real-time simulation results and the PSCAD/EMTDC simulation results, the higher the simulation accuracy.

The parameters of the four-terminal converters are shown in Table 2. $MMC_1$, $MMC_2$, and $MMC_4$ use active power control and reactive power control, while $MMC_3$ uses DC voltage control and reactive power control.

The interface transformer of RTDS is equipped with line-to-ground damper branches to be connected on the primary side, including a resistive branch and aseries RC branch. The typical values of the damper branches are shown in Table 3.

### 5.1 | Time and space properties

The version of PSCAD/EMTDC is V5.0.0, running on the server with 3.10 GHz 20-core CPU and 128 GB memory, whose operating system is Windows Server 2016.

The software of RTDS is RSCAD 5.012, the hardware of RTDS is NovaCor and MMC Support Unit V2. The MMC Support Unit V2 is composed of the Xilinx VC707 development kit, which is the same as the developed simulator. Therefore, comparing the resource consumption of the MMC Support Unit V2 and the developed simulator can better reflect the differences in the space property between the developed simulator and existing real-time simulator.

The RTDS platform is shown in Figure 11. Each terminal of MMC-HVDC is simulated on one NovaCor separately. The MMC Support Unit V2 is used to achieve valve calculation and capacitor voltage balancing control of the positive pole converter of $MMC_4$.

In terms of resource consumption, according to the manuals of RTDS, $Unit_1$ of the MMC Support Unit V2 is used to achieve the valve calculation of six arms of the positive pole converter of $MMC_4$, $Unit_2$ is used to achieve capacitor voltage balancing control of upper arms, and $Unit_3$ is used to achieve capacitor voltage balancing control of lower arms.

However, the developed simulator uses only one unit to achieve the complete simulation of single-terminal true bipolar MMC. Therefore, the resource consumption of the developed simulator is much lower than that of the RTDS platform.

In terms of the simulation speed, when the simulation duration is 1 s, the running time of PSCAD/EMTDC is 1630 s, while the running time of the developed simulator and RTDS platform are both 1 s, indicating that the simulation speed of the real-time simulator is much higher than that of off-line simulation software.

In addition, the minimum step for small-step simulation on RTDS is 1.4 μs. According to Table 1, the computing time of the primary system on the developed simulator is 1.69 μs at a clock frequency of 100 MHz, while the clock frequency of the simulator can reach up to 200 MHz. Therefore, the theoretical minimum step on the developed simulator is smaller than 1.4 μs, indicating that the simulation speed of the developed simulator is faster than that of the RTDS platform.

### 5.2 | Dynamic-state simulation

We set the initial value of the SM capacitor voltage to 2 kV and started the converter at each terminal under deblocking when $t = 0$. Considering the symmetry of the simulation system, we used the simulation results of the positive pole converter of $MMC_4$ as an example of the proposed method's accuracy. The simulation results during startup are shown in Figure 12, which is followed by the DC voltage, DC current, and A-phase arm current from top to bottom.

**TABLE 2** Parameters of the simulation system.

| Converter | Item | Value | Item | Value |
|---|---|---|---|---|
| $MMC_1$ | Transformer ratio | 525/290.88 | Transformer capacity (MVA) | 1700 |
| | Leakage reactance (pu) | 0.18 | Rated active power (MW) | 3000 |
| | Rated reactive power (Mvar) | 0 | Rated DC voltage (kV) | ±500 |
| | Arm reactance (H) | 0.05 | Number of SMs | 244 |
| | Capacitor of SM (F) | 0.015 | AC impedance ($R//L$) (Ω) | 10.75∠80° |
| $MMC_2$ | Transformer ratio | 230/290.88 | Transformer capacity (MVA) | 1700 |
| | Leakage reactance (pu) | 0.16 | Rated active power (MW) | 3000 |
| | Rated reactive power (Mvar) | 0 | Rated DC voltage (kV) | ±500 |
| | Arm reactance (H) | 0.05 | Number of SMs | 244 |
| | Capacitor of SM (F) | 0.015 | AC impedance ($R//L$) (Ω) | 2.06∠80° |
| $MMC_3$ | Transformer ratio | 525/290.88 | Transformer capacity (MVA) | 850 |
| | Leakage reactance (pu) | 0.15 | Rated active power (MW) | 1500 |
| | Rated reactive power (Mvar) | 0 | Rated DC voltage (kV) | ±500 |
| | Arm reactance (H) | 0.1 | Number of SMs | 244 |
| | Capacitor of SM (F) | 0.008 | AC impedance ($R//L$) (Ω) | 21.5∠80° |
| $MMC_4$ | Transformer ratio | 230/290.88 | Transformer capacity | 850 |
| | Leakage reactance (pu) | 0.15 | Rated active power | 1500 |
| | Rated reactive power (Mvar) | 0 | Rated DC voltage | ±500 |
| | Arm reactance (H) | 0.1 | Number of SMs | 244 |
| | Capacitor of SM (F) | 0.008 | AC impedance ($R$) (Ω) | 2 |
| DC line | Resistance (Ω/m) | $0.1\times e^{-4}$ | Inductive reactance (Ω/m) | $0.16\times e^{-5}$ |
| | Capacitive reactance (MΩm) | $1.3\times e^{5}$ | $MMC_1$ to $MMC_2$ (km) | 208.4 |
| | $MMC_1$ to $MMC_3$ (km) | 189.1 | $MMC_2$ to $MMC_4$ (km) | 49.6 |
| | $MMC_3$ to $MMC_4$ (km) | 207.1 | —— | —— |

Abbreviations: MMC, modular multilevel converter; SM, sub-module.

**TABLE 3** Parameters of damper branches.

| Item | Value |
|---|---|
| Resistive branch, $R$ (Ω) | 31,117.647 |
| Series RC branch, $R$ (Ω) | 244.397 |
| Series RC branch, $C$ (nF) | 102.292 |

As shown in Figure 12, there was some deviation between the instantaneous values of electrical quantities under off-line simulation and real-time simulation conditions. However, the trends of electrical quantities are basically the same, and the error between the results for the PSCAD/EMTDC and the results for the developed simulator is obviously smaller than the error between the results for the PSCAD/EMTDC and the results for the RTDS simulator. Based on the simulation results of the PSCAD/EMTDC, the root mean square error of the arm current for the developed simulator is 0.0269 kA.

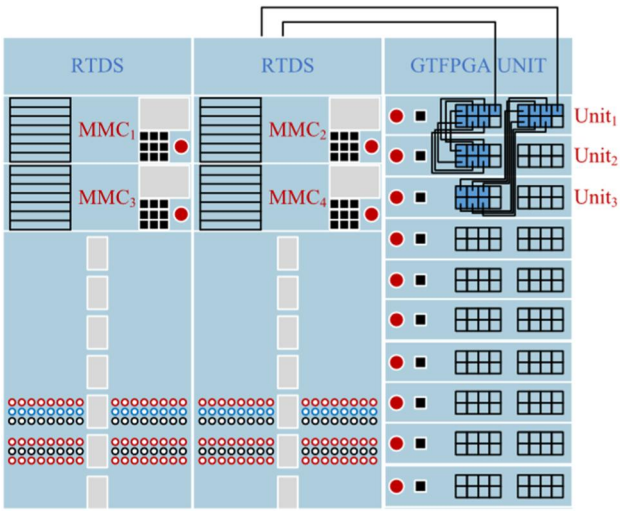


**FIGURE 11** Real time digital simulator (RTDS) platform.

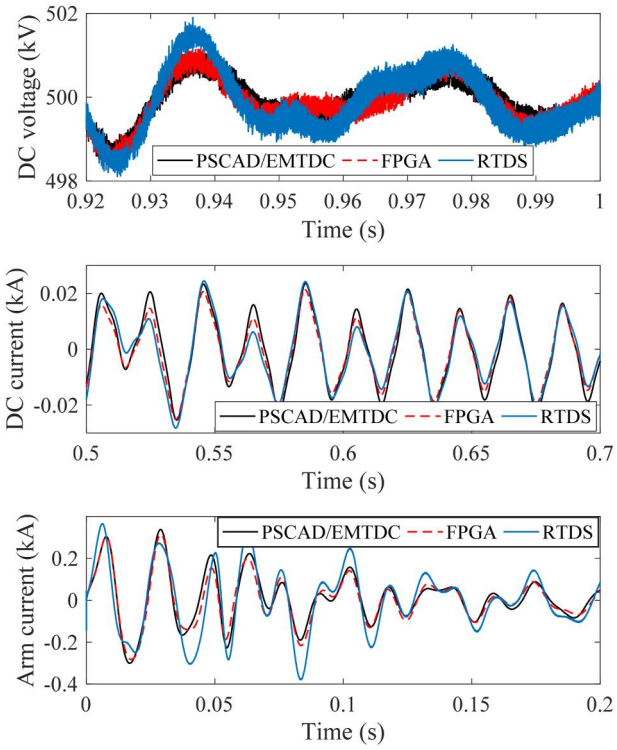


**FIGURE 12** Dynamic-state simulation.

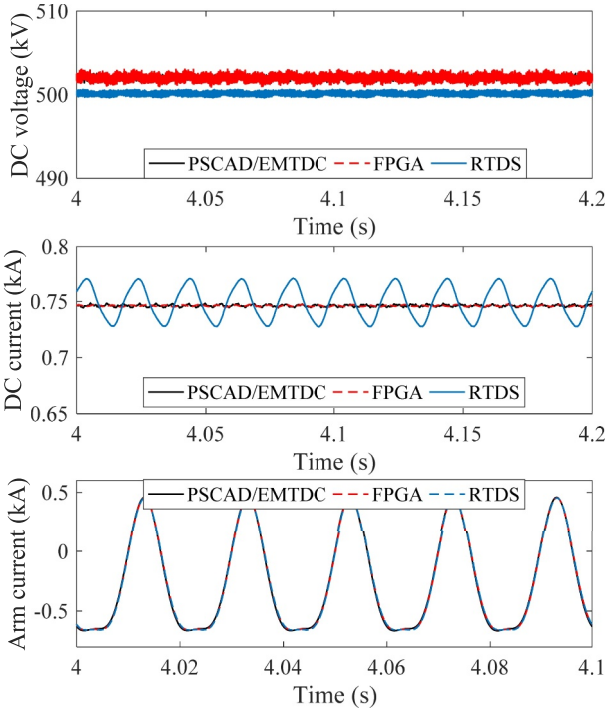


**FIGURE 13** Steady-state simulation.

## 5.3 | Steady-state simulation

Next, we set the reference of active power of each converter as half of the rated value. Figure 13 shows the comparison of simulation results in the steady state. The results of the positive pole converter of $MMC_4$ are shown in Figure 13 as an example, with the DC voltage, DC current, and A-phase arm current from top to bottom. The instantaneous values of each electrical quantity under the steady state of the PSCAD/EMTDC and the developed real-time simulator are basically consistent, while the error between the PSCAD/EMTDC and the RTDS platform is large. Based on the simulation results of the PSCAD/EMTDC, the root mean square error of the arm current for the developed simulator is 0.012 kA.

## 5.4 | Frequency sweep

### 5.4.1 | Influence of simulation step on accuracy

We added the harmonic voltage source to the AC-side network of the converter, measured the AC voltage and current at the primary side of the converter transformer, calculated the MMC impedance-frequency curve, and compared it with the theoretical model of MMC impedance-frequency characteristics to verify the accuracy of high-frequency impedance in the simulation system. The control link delay in this case was 300 μs.

The frequency sweep results are shown in Figure 14, where the blue solid line marks the theoretical model of the MMC high-frequency impedance drawn according to Equation (6), and the red dotted line is the MMC high-frequency impedance obtained based on the frequency sweep of the PSCAD/EMTDC. The red

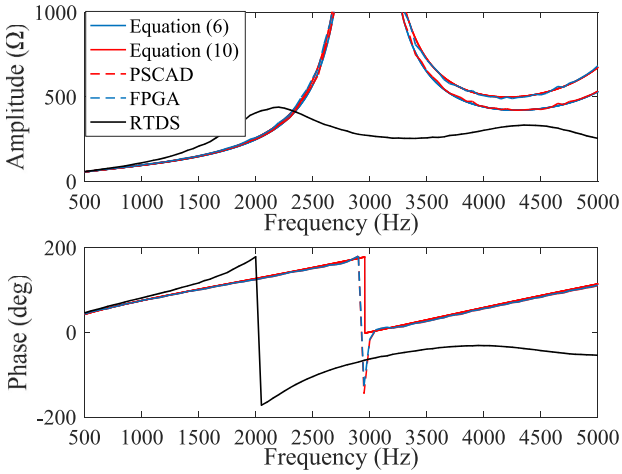


**FIGURE 14** Simulation step effects.

solid line is the theoretical model of MMC high-frequency impedance corrected according to Equation (10), taking into account the influence of simulation steps. The blue dotted line is the MMC high-frequency impedance obtained based on the frequency sweep of the developed simulator. The black solid line is the MMC high-frequency impedance obtained based on the frequency sweep of the RTDS.

As shown in Figure 14, the impedance characteristics of the MMC on the large-step side in the developed multi-rate simulator had an amplitude error in the high-frequency band. This is consistent with the error obtained from our theoretical analysis, and the error is acceptable.

Due to the network partition method and the damper branches connected on the primary side of the RTDS interface

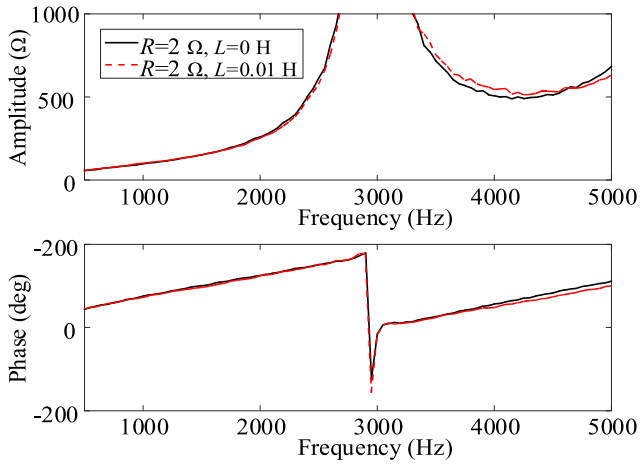


**FIGURE 15** Influence of alternating current (AC) network.

transformer model, the impedance characteristics of the MMC on the large-step side in the RTDS platform have significant errors, which will have a significant impact on the analysis of the high-frequency resonance of the MMC connected to the AC network.

### 5.4.2 | Influence of alternating current network on accuracy

We changed the value of inductance in the AC-side network of $MMC_4$ and tested the influence of the AC network on multi-rate simulation accuracy based on the frequency sweep. The results are shown in Figure 15. The high-frequency impedance characteristics of the MMC deviate to greater extent as the inductance value in the large-step network increases, which confirms our findings from Section 4.2.

## 5.5 | High-frequency resonance

To test the role of the developed real-time simulation platform in the analysis of high-frequency resonance, we established a simple AC system as shown in Figure 16. This system was connected to the AC bus of $MMC_4$. The parameters of the AC system are listed in Table 4.

We set $T_d = 300$ μs and simulated N-1 fault in the AC system when $t = 4.5$ s. The simulation results after the fault are shown in Figure 17. The A-phase voltage and its harmonics on the AC side of $MMC_4$ are shown from top to bottom. The high-frequency resonance appears to occur after the fault, with a frequency of 2550 Hz. The simulation results for the PSCAD/EMTDC are basically consistent with the real-time simulation results of the developed FPGA-based simulator. The harmonics of the A-phase voltage obtained by the Fourier transform are also roughly the same, which indicates that the developed FPGA-based real-time simulation platform can be used to analyse the high-frequency resonance of the MMC connected to the AC network.

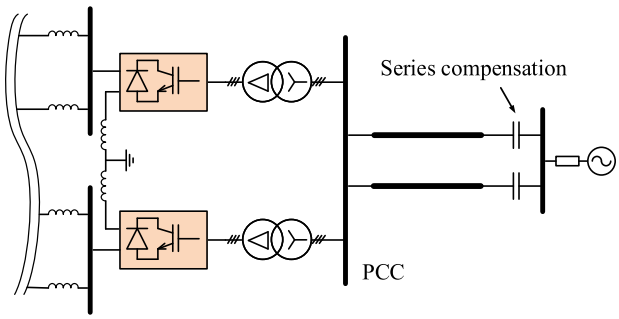


**FIGURE 16** Topology of alternating current (AC) system.

**TABLE 4** Parameters of the alternating current (AC) system.

| Item | Value | Item | Value |
|---|---|---|---|
| Source resistance (Ω) | 0.75 | Line resistance (Ω/km) | 0.03 |
| Series compensation (μF) | 200 | Line inductance (mH/km) | 0.9 |
| Line length (km) | 100 | Line capacitance (nF/km) | 1.3 |

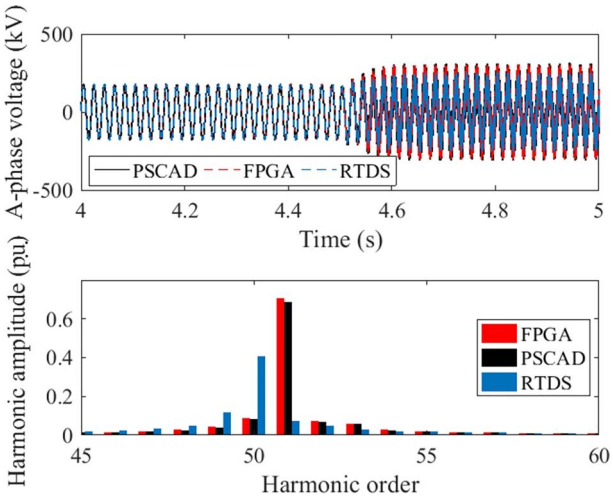


**FIGURE 17** High-frequency resonance.

Due to the significant errors for the high-frequency impedance characteristics of MMC in the RTDS platform, the resonance of MMC based on the RTDS platform does not match the theoretical result. There are significant differences in the resonance frequency and amplitude.

The above test results indicate that the simulation accuracy, simulation speed, and resource utilisation of the developed FPGA-based real-time simulator have significantly improved, all of which are better than those of the RTDS platform.

## 6 | CONCLUSION

In this study, we proposed a parallel multi-rate simulation scheme for the MMC-HVDC suitable for analysing high-frequency resonance characteristics. We constructed a real-time simulation platform of the four-terminal true bipolar MMC-HVDC based on the FPGA. We compared its real-time

simulation results with PSCAD and RTDS simulation results. Our conclusions can be summarised as follows.

(1) The proposed parallel multi-rate simulation scheme can achieve decoupling among converters, within converters, and between the converter and AC system while ensuring accurate simulation of high-frequency characteristics. It can be applied for real-time simulation of the MMC-HVDC.
(2) The established real-time MMC-HVDC simulation platform based on the FPGA can optimise resource consumption and enhance simulation efficiency. One FPGA can realise the solution of the primary system and calculation of the control system of a 257-level single-terminal true bipolar MMC.
(3) In cases of multi-rate simulation, there are some errors in the high-frequency characteristics of the MMC which are mainly caused by the simulation step and inductive, capacitive, and controlled elements of the large-step network. The former has less influence on the high-frequency impedance characteristics and can be quantified. The latter is difficult to quantify due to the structure, parameters, and other factors. Further research is needed to mitigate this error.

## ACKNOWLEDGEMENTS

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## CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

## DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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## REFERENCES

1. Sun, J., et al.: Renewable energy transmission by HVDC across the continent: system challenges and opportunities. CSEE J. Power Energ. Syst. 3(4), 353–364 (2017)
2. Dong, X., et al.: Confronting problem and challenge of large-scale AC-DC hybrid power grid operation. Proc. CSEE 39(11), 3107–3119 (2019). (in Chinese)
3. Dong, Y., et al.: Review of high efficiency digital electromagnetic transient simulation technology in power system. Proc. CSEE 38(8), 2213–2231 (2018). (in Chinese)
4. Dekka, A., et al.: Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters. IEEE J. Emerg. Sel. Top. Power Electron. 5(4), 1631–1656 (2017)
5. Wang, J., et al.: Steady-state power operation region of a modular multilevel converter connecting to an AC grid. High Volt. 6(6), 1009–1023 (2021)
6. He, Z., et al.: Modelling and analysis of half-/full-bridge hybrid MMC when riding through DC-side pole-to-ground fault. High Volt. 7(3), 496–509 (2022)
7. Buchhagen, C., et al.: BorWin1-First experiences with harmonic interactions in converter dominated grids. In: Proceedings of International ETG Congress, pp. 17–18. Bonn (2015)
8. Yin, C., et al.: Analysis and control of the oscillation phenomenon in VSC-HVDC transmission system. Power Syst. Technol. 42(4), 1117–1123 (2018). (in Chinese)
9. Ou, K., et al.: MMC-HVDC simulation and testing based on real-time digital simulator and physical control system. IEEE J. Emerg. Sel. Top. Power Electron. 2(4), 1109–1116 (2014)
10. Saad, H., et al.: Real-time simulation of MMCs using CPU and FPGA. IEEE Trans. Power Electron. 30(1), 259–267 (2015)
11. Xu, Z., et al.: A review of parallel computing digital simulation of large-scale AC/DC power systems. Electric Power Construction 37(2), 1–9 (2016). (in Chinese)
12. Hui, S., et al.: Decoupled simulation of multi-stage power electronic systems using transmission-line links. In: Power Electronics Specialists Conference, pp. 1–7. Toledo (1992)
13. Ilic, M., et al.: Transient stability simulation by waveform relaxation methods. IEEE Trans. Power Syst. 2(4), 943–952 (1987)
14. Armstrong, M., et al.: Multilevel MATE for efficient simultaneous solution of control systems and nonlinearities in the OVNI simulator. IEEE Trans. Power Syst. 21(3), 1250–1259 (2006)
15. Mu, Q., et al.: A parallel multi-rate electromagnetic transient simulation algorithm based on network division through transmission line. Autom. Electr. Power Syst. 38(7), 47–52 (2014). (in Chinese)
16. Lelarasmee, E., Ruehli, A., Sangiovanni-Vincentelli, A.: The waveform relaxation method for time-domain analysis of large-scale integrated circuits. IEEE Trans. Comput. Aided Des. Integrated Circ. Syst. 1(3), 131–145 (1982)
17. Schutt-Aine, J.E.: Latency insertion method for the fast transient simulation of large networks. IEEE Trans. Circuit Syst. 48(1), 81–89 (2001)
18. Crow, M., Ilic, M.: The parallel implementation of the waveform relaxation method for transient stability simulations. IEEE Trans. Power Syst. 5(3), 922–932 (1990)
19. Burrage, K., et al.: Acceleration of convergence of static and dynamic iterations. BIT Numer. Mathemat. 41(4), 645–655 (2001)
20. Pruvost, F., et al.: Speed-up the computing efficiency of waveform relaxation method for power system transient stability. In: Proceedings of the first international workshop on High performance computing, networking and analytics for the power grid, Seattle, USA, pp. 11–18, (2011)
21. Benigni, A., Monti, A., Dougal, R.A.: Latency-based approach to the simulation of large power electronics systems. IEEE Trans. Power Electron. 29(6), 3201–3213 (2014)
22. Milton, M., Benigni, A.: Latency insertion method based real-time simulation of power electronic systems. IEEE Trans. Power Electron. 33(8), 7166–7177 (2018)
23. Ding, H., et al.: Device-level multi-rate electromagnetic transient simulation of power systems based on latency insertion method. In: 2022 7th Asia Conference on Power and Electrical Engineering, pp. 1–5. Hangzhou (2022)
24. Tomim, M., Marti, J.R., Passos Filho, J.A.: Parallel transient stability simulation based on multi-area Thevenin equivalents. IEEE Trans. Smart Grid 8(3), 1366–1377 (2017)
25. Han, J., et al.: Multi-rate and parallel electromagnetic transient simulation considering nonlinear characteristics of a power system. Energies 11(2), 468 (2018)
26. Zhai, X., et al.: Multi-rate real-time simulation of modular multilevel converter for HVDC grids application. In: 43rd Annual Conference of the IEEE Industrial Electronics Society, pp. 1–6. Beijing (2017)
27. Wang, P., et al.: Digital-analog hybrid simulation of large-scale AC-DC power grids based on ADPSS next-generation simulation platform. Power Syst. Technol. 45(1), 227–234 (2021). (in Chinese)
28. Li, Q., et al.: Analysis and comparison on modeling method of cascade SVG based on RTDS. Power Capacit. React. Power Compens. 37(3), 45–50 (2016). (in Chinese)
29. Saad, H., et al.: Real time simulation of MMCs using the state-space nodal approach. In: The International Conference on Power Systems Transients, pp. 1–7. Vancouver (2013)
30. Ou, K., et al.: Research and application of small time-step simulation for MMC VSC-HVDC in RTDS. In: 2014 International Conference on Power System Technology, pp. 1–6. Chengdu (2014)
31. Bartel, A., Günther, M.: A multirate W-method for electrical networks in state–space formulation. J. Comput. Appl. Math. 147(2), 411–425 (2002)

32. Moreira, F., et al.: Multirate simulations with simultaneous-solution using direct integration methods in a partitioned network environment. IEEE Trans. Circuits Syst. Regular Pap. 53(12), 2765–2778 (2006)
33. Ou, K., et al.: Research on the Multi-Time Scale Real-Time Hybrid Simulation Technologies for AC/DC Large-Scale Power Grid and its Engineering Application. South China University of Technology, Guangzhou (2017)
34. Hou, Y., et al.: Mechanism analysis of additional damping control strategies for the high-frequency resonance of MMC connected to AC grid. CSEE J. Power Energ. Syst. 9(3), 1173–1181 (2023)
35. Dommel, H.W.: EMTP Theory Book, pp. 12. Water Resources and Electric Power Press (1986)

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